A 100nA Cardiac Sensing Channel

Author: Rafael Puyol

Tutor: Matias Miguez
Master of Science in Electrical Engineering
Department of Electrical Engineering
Faculty of Engineering and Technologies - Universidad Católica del Uruguay

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Abstract

Implantable medical devices first appeared in the 1970s [1] and performed simple tasks, the first pacemakers could only stimulate the heart at a fixed rate without any biological feedback. With the progress of technology, especially microelectronics, new features have been added. Sensing the heart activity soon became a requirement, allowing to save battery by stimulating the heart only when needed and at the same time providing a better therapy for the subject. Every modern pacemaker includes a sensing circuit, this circuit is working all the time. For this reason reducing its consumption can extended the duration of the battery for much longer. Taking into account the work available there is an opportunity to design a sensing channel with much lower consumption that those published to date.

This work presents the design of 100nA cardiac sensing channel for pacemaker applications with a supply voltage ranging from 2V up to 3.2V. It is designed in a 0.6μm high voltage CMOS technology. The sensing channel must generate a digital pulse when a heartbeat is detected. The circuit contains a Gm-C bandpass filter to adapt and amplify the cardiac signal followed by a comparator to make the detection and additional circuitry to control gain and offset of the filter. Several low power techniques are used, like adaptive bias current and digital offset trimming.

The design is validated with simulations, using the standard Tokyo test signal, proposed by [2]. Relevant parameters such as: gain, offset, current consumption, stability and noise are also measured. Montecarlo simulations are done to asses the variability of the circuit with uncertainties introduced in the manufacturing process. Finally a physical layout for the manufacturing on the mentioned technology is included. The layout area is 0.79 mm^2 and layout techniques to minimize mismatch were extensively used. The integrated circuit will soon be manufactured and tested.

Keywords: Cardiac Sensing, Implantable Devices, Low Power, Pacemaker.

Contents

Chapter 1

Introduction

1.1 Problem statement

The cardiovascular system of every human being has a pumping station, the heart. It is a conically shaped hollow muscular organ with an average weight of 325g [3]. Its size is 12 to 13 cm from base to top and 7 to 8 cm wide [3] and has an internal muscular wall which divides its two sides. Each side, which is a self-contained pumping station, is composed by two chambers, called atrium and ventricle [3]. One side of the heart drives oxygen-rich blood and the other drives the oxygen-poor blood. The pumping process is rhytmic, and its frequency is dependent on the oxygen need of the cells, among other factors. In the right atrium there is a neuromuscular tissue called Sinoatrial (SA) node. The SA node produces electrical impulses that trigger the heartbeat acting as a natural pacemaker. A dysfunction of the SA node produces an irregular or aperiodic heartbeat, this condition is known as arrhythmia.

Bradycardia is a type of arrhythmia in which the heart beats slower than it should, below 60bpm [4]. It can also be in an aperiodic fashion. This condition causes a feeling of malaise in the subject and deteriorates his body functions.

A pacemaker is an implantable electronic device designed to stimulate the heart and treat bradycardia. First implantable pacemakers appeared in the 1970s and with the advancements of technology more functions were progressively added [1].

Modern pacemakers sense the heart activity searching for a missing heartbeat, if needed an electrical pulse is applied to the heart muscle to trigger a heartbeat. Modern devices are typically dual-chamber, they sense electrical activity in the ventricle and atrium of the right side of the heart to see if pacing is needed. This technique requires two leads, one placed in the atrium and the other in the ventricle. When pacing is needed the excitation of both chambers is synchronized to mimic normal heart activity. Every pacemaker has some sort of sensing and stimulation stages. A general diagram of a pacemaker is shown in Figure 1.1. Modern pacemakers are complex implantable devices which integrate many extra features, like data logging, telemetry as well as measurement of other body parameters to improve the pacing strategy.

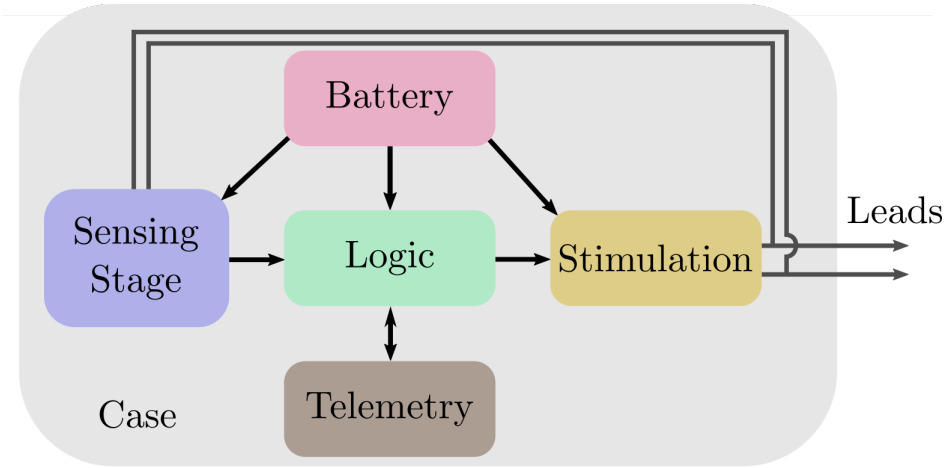


Figure 1.1: General diagram of a modern pacemaker.

The device is usually implanted near the shoulder and connected to the heart through electrodes as shown in figure 1.2. Recently a new type of pacemaker was developed by Medtronics plc, which is implanted directly inside the heart [19]. The method of implantation is different for both types, the former requires more invasive surgery while the latter is implanted transcatheter.

All the components of a pacemakers, except for the leads, are cased in a titanium box for biocompatibility. If the primary battery (non-rechargeable) that powers the system drains, a surgery must be performed to replace the pacemaker with a new one. Therefore it is desirable to decrease the pacemaker consumption in order to extend the battery life. Typically the battery life is around 10 years but it heavily depends on the demand for stimulation [1].

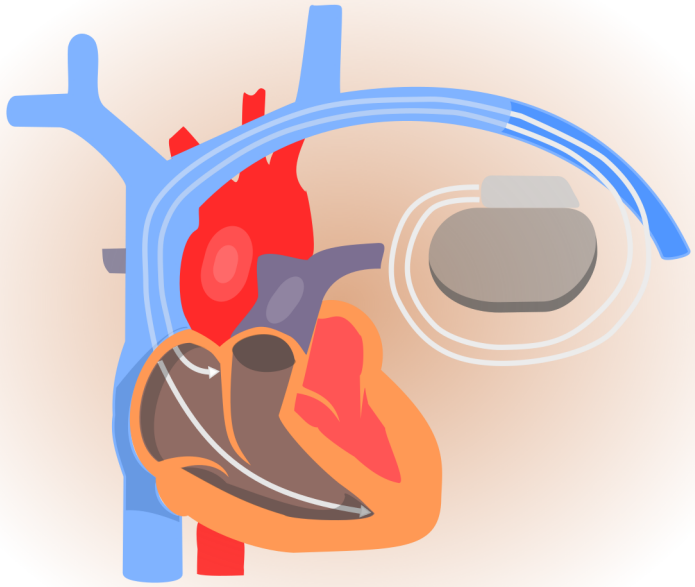


Figure 1.2: Implanted pacemaker.

Lithium-Iodine batteries are preferred due to its high energy density and well known behaviour [5]. The pacemaker must perform properly throughout the whole life cycle of the battery. Even though its nominal voltage is 2.8V the voltage drops as the battery is discharged and it is around 2V when the battery is near the end of life [5].

Several efforts have been made to decrease the power consumption of every circuit in a pacemaker. An area where further optimization is feasible is the sensing stage. Leaving aside the stimulation block whose consumption depends heavily on the subject condition, the sensing channel is the block with the largest consumption.

The objective of this work is to design a sensing stage for a pacemaker capable of detecting heartbeats as described by the international standard for pacemakers [2] and with a current consumption under 100nA on average. Although no higher voltages than 2.8V are expected the circuit is designed to operate properly up to 3.2V.

The sensing channel should include at least a bandpass amplifier to filter out interference and noise as well as a comparator to detect a heartbeat. There is a tradeoff between the

amplifier and the comparator requirements. In this work the design of the comparator is more challenging than that of the filter so the filter requirements are defined after the comparator has been sketched. For the comparator the design of Isono et al [22] is chosen as a starting point and tuned for the application. An initial diagram of the sensing channel is shown in figure 1.3.

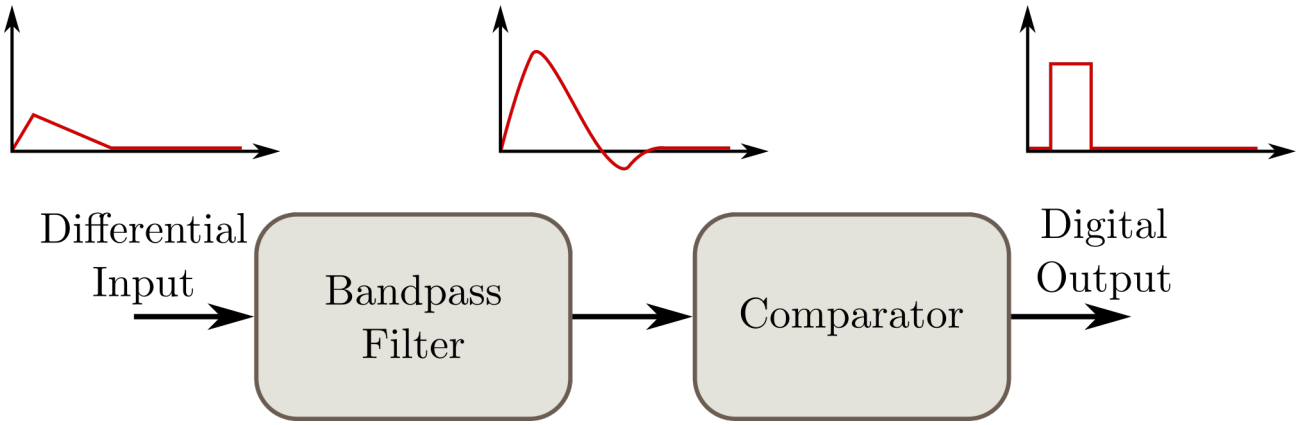


Figure 1.3: Sensing channel.

The different components of the sensing channel are studied in the following chapters, figure 1.4 shows a schematic with all the inputs and outputs of every block and how they relate.

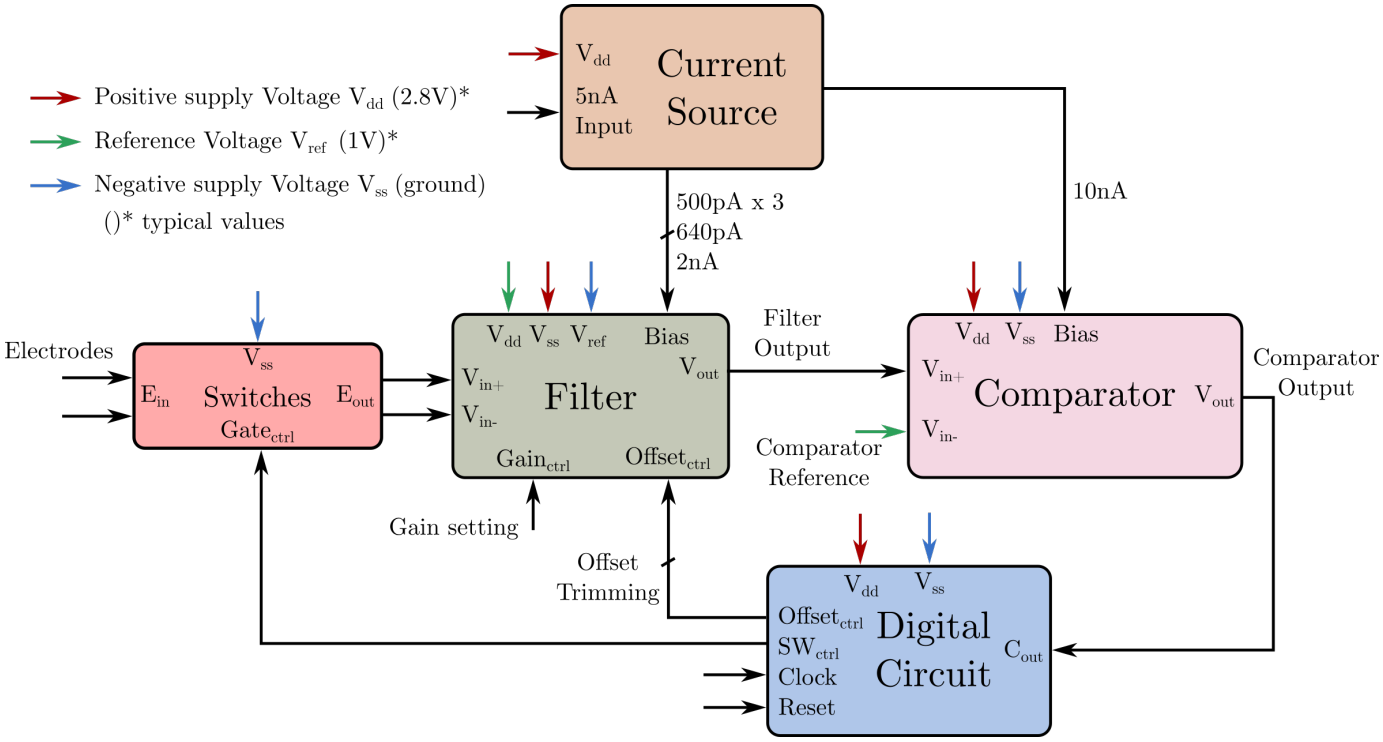


Figure 1.4: Sensing channel.

1.2 Requirements

The objective is to design a sensing channel with an average current consumption below 100nA which complies with [2]. To assess pacemakers performance the standard Tokyo test signal proposed by [2] is designed. It is a periodic triangle signal with a rise time of 2ms and a fall time of 13ms. The period is in the range of the heartbeat found on a human heart. The proposed design must be tested with simulations taking into account the technological process variations.

Besides the design of the circuit it is also required to design the layout of the integrated circuit to be built with a standard HV CMOS process, to be later manufactured and tested.

1.3 Low Power Design

The need for longer battery life and the widespread of portable and wireless electronic devices has lead to development of circuit design techniques aimed at reducing power consumption, without sacrificing performance. The characteristics of a circuit: speed, bandwidth, power consumption, linearity, are always interwoven. There is usually a trade-off between bias current and performance, this is not a problem as long as the deterioration is on the most relaxed characteristics. A dynamic adjustment of the operating state to meet sporadic performance demands is desirable.

From a device perspective, CMOS transistors can operate in three regions of inversion, weak, moderate and strong. Being strong the most power hungry. Physical models that cover all three regions of inversion, from weak to strong, have been developed [23]. Throughout the last decades weak inversion has gained attention, in this region transistors are more efficient at generating transconductance than in strong inversion. On the other hand electrical noise has a larger impact on circuits biased in weak inversion.

The technological process also plays a role in the efficiency of a circuit, the transconductance of transistors, leakage currents and noise depend on it. Unfortunately there is not much room for improvement in this aspect given the actual CMOS processes available.

1.4 Safety

The input of the circuit is connected directly to the electrodes which are inserted in the heart. A failure or current leakage could prove fatal for the subject or cause severe damage therefore it is mandatory to apply safe design rules especially for the input circuit. No single fault can cause damage to the patient, this does not mean that the pacemaker will continue to operate as it should [2]. A constant DC current through the heart tissue larger than a few microamperes can damage the muscles and put the life of the subject under threat. During the schematic and layout of the circuits, this was taken into consideration. Nevertheless most Pacemaker include decoupling capacitors in series with the leads, giving an extra layer of protection.

The structure of the document is as follows. First the circuit is explained starting with the comparator, then the filter, the current sources and the digital circuit. A chapter with simulations of the whole circuit follows, the next is dedicated to the layout. At the end there are the conclusions and some ideas for future work.

Chapter 2

Circuit Design

2.1 Comparator

This section deals with the analysis and simulation of the comparator. Comparators can be classified into two main categories: continuous and clocked or latched. A continuous will permanently output a digital signal according to the sign of the differential input voltage. A clocked comparator will behave in the same way but the comparison is only performed when a trigger signal is applied and the output is held constant [6]. Clocked comparators require an external digital clock, for this reason it has been chosen to use a continuous time one.

The organization of this section is as follows: firstly Adaptive Bias Current Generation (ABCG), which is used in the design will be explained, then the comparator is presented and finally some modifications to solve unwanted behaviour are added.

2.1.1 Adaptive Bias Current Generator

ABCG was designed to deal with the compromise between bias current and slew rate in amplifiers when subjected to large input signals. This is especially important when working in low power designs biased in weak inversion, as little current is available. ABCG is used in amplifier design to implement a variable bias current which depends on the disturbance of the input signal from the virtual ground. Current subtractors are used to achieve this variable

current.

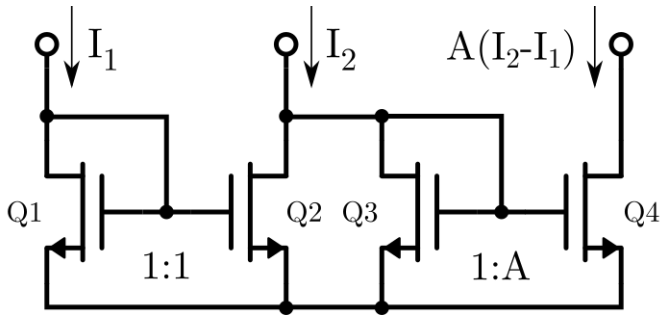


Figure 2.1: Current subtractor.

Figure 2.1 presents a current subtractor, the output current is $A|I_2 - I_1|$ as long as I2 is larger than I1 otherwise it is zero. The factor A is the quotient of width to length ratios of Q3 and Q4. This circuit can be used to implement a variable bias current if currents I_1 and I_2 are somehow related to the input signal. For example two subtractors can be used to achieve ABCG in an input differential pair as presented in figure 2.2.

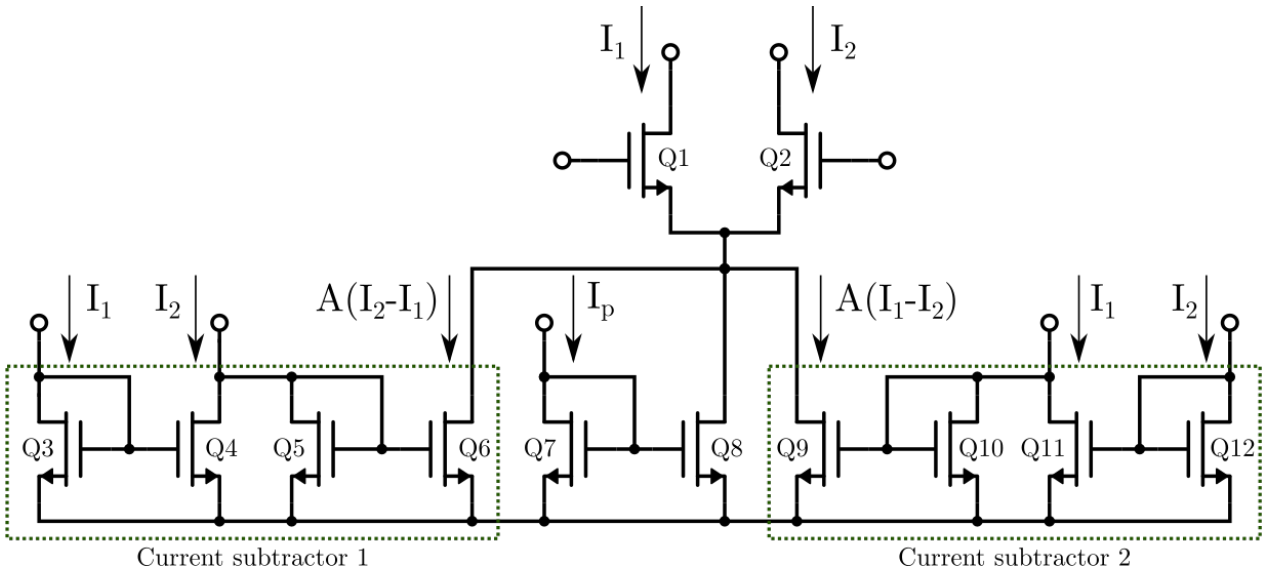


Figure 2.2: ABCG differential amplifier.

I_p is a fixed bias current, I_1 and I_2 are the currents at the drain of Q1 and Q2 respectively. Current mirrors not shown in the schematic copy I_1 and I_2 to feed the current subtractors 1 and 2. The total bias current of the differential pair is then $I_p + A|I_1 - I_2|$ which is an input dependent bias current as desired. A more detailed description of the effects of A on the slew rate can be seen in [21]. This variable bias current differential pair is designed for amplifiers but can be used for a comparator input stage as well, as explained in the following subsection.

2.1.2 Design

A high end comparator typically contains three stages. First, there is a transconductance preamplifier to improve sensitivity, usually implemented with a differential pair. A decision circuit follows, this is a positive feedback network that is sensitive to the current difference produced by the preamplifier. It must detect signals in the mV range and have some hysteresis to reject noise. The output buffer generates the digital output signal [15], figure 2.3.

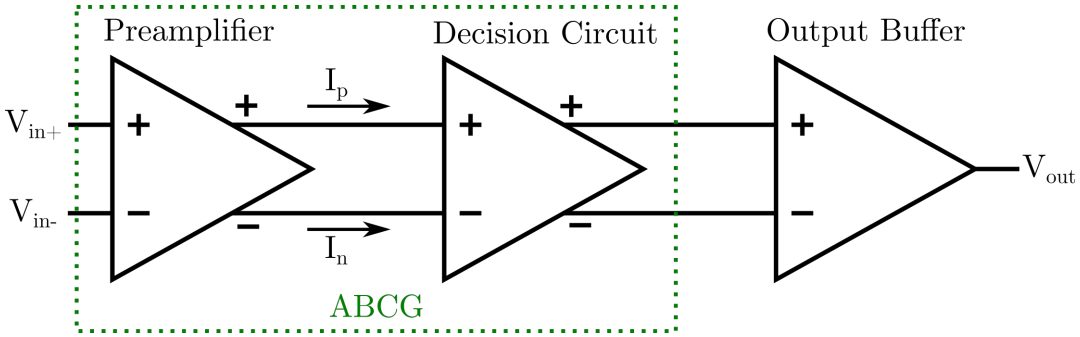


Figure 2.3: Basic structure of a comparator.

The selected comparator design is very similar to that proposed by Isono et al [22], which follows the classical comparator topology mentioned above but takes advantage of ABCG to achieve an extremely low power consumption while retaining high speed and low offset. The schematic is presented in figure 2.4.

The preamplifier is a PMOS differential pair implemented by transistors Q1 and Q2 biased in weak inversion. The preamplifier takes advantage of ABCG to achieve a variable bias current. While the differential input voltage is zero, ABCG is turned off and the bias current for each transistor is 5nA. Otherwise ABCG is turned on and the bias current increases. The area of both transistors has been optimized to reduce mismatch and at the same time have a low enough input capacitance.

Transistors Q3, Q4, Q6 and Q8 make the decision circuit (outlined in red) which adds positive feedback. If the differential input voltages is zero, $I_{ref}/2$ flows out of Q1 and Q2 drains. If Vin- decreases, the current I_1 increases. Therefore the voltage at the drain of Q4 increases so Q3 turns on and the voltage at the drain of Q3 decreases turning Q4 off. This causes all the current flowing through Q1 to go through Q6 and the current through Q2 to enter Q3 and Q8 as depicted by the simulation in Figure 2.5.

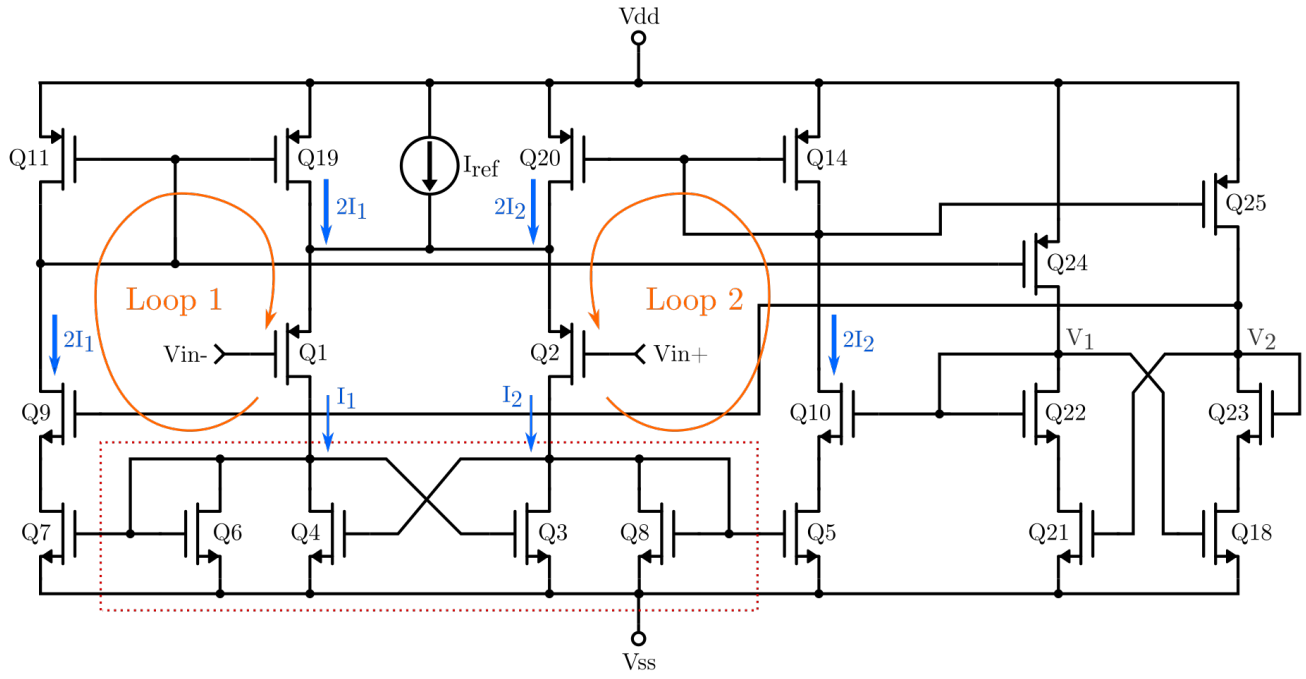


Figure 2.4: Comparator schematic.

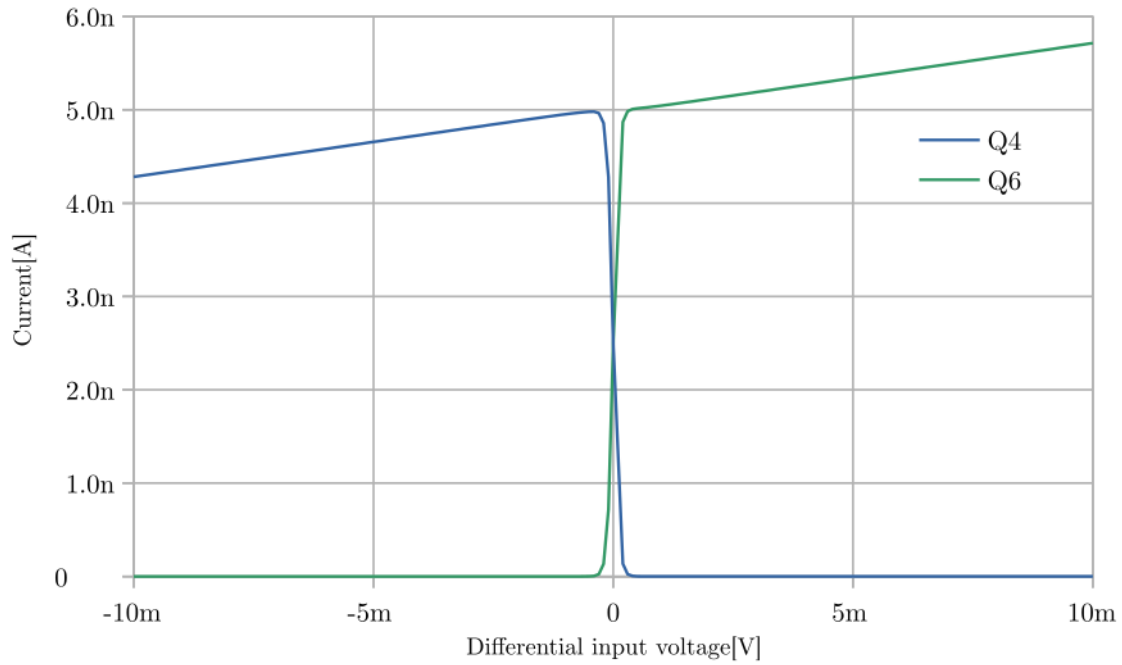


Figure 2.5: Decision circuit performance.

Two positive feedback loops, denoted Loop 1 and Loop 2, implement the ABCG for the input differential pair in the same fashion as explained in the previous subsection for the amplifier. The transistors involved in Loop 1 are: Q6, Q7, Q11, Q19 and those in Loop 2: Q8, Q5, Q20, Q14. Q6 and Q7 have the same length but different width, their ratio is denoted K,

so the current flowing in Q7 is K times that flowing in Q6. The current flowing out of Q19 or Q20 is called the adaptive current.

Q9 and Q10 are switches driven by an output latch, never are both in the same state, their purpose is to stop the adaptive current in the inactive loop.

In the active loop the current flowing through the input transistor, Q1 or Q2 is in the range $0.5Iref < I1 < Iref$ at first, when the adaptive current is not taken into account. If the adaptive current is added, considering the process as a continuous time iteration, the total bias current becomes:

$$I_{bias} = \alpha I_{ref}(1 + K + K^2 + ...) \tag{2.1}$$

K is chosen to be 2 so the bias current becomes ideally infinity, although this does not happen in reality.

To analyze the behavior of the comparator it is better to study the 4 possible cases separately, referred to figure 2.4:

1. Positive input voltage, V_1 = Low, V_2 = High.
2. Positive input voltage, V_1 = High, V_2 = Low.
3. Negative input voltage, V_1 = Low, V_2 = High.
4. Negative input voltage, V_1 = High, V_2 = Low.

Case 1

In this case the current through Q1 is larger and as V2 is high Q9 is turned on. The adaptive current in L1 will be generated. As Q24 copies the current flowing out of Q11 it will make the latch switch its state. This in turns makes Q9 to turn off and a new equilibrium state is achieved

Case 2

In this case the current through Q1 is larger and Q9 is turned off so the adaptive current will not be generated and the latch will remain as it is.

Case 3

In this case the current through Q2 is larger and Q10 is turned off so the adaptive current will not be generated and the latch will remain as it is.

Case 4

In this case the current through Q2 is larger and as V1 is high Q10 is turned. The adaptive current in L2 will be generated. As Q25 copies the current flowing out of Q14 it will make the latch switch its state. This in turns makes Q10 to turn off and a new equilibrium state is achieved.

Input	Previous V1	Next V1
Positive	Low	High
Positive	High	High
Negative	Low	Low
Negative	High	Low

Table 2.1: Comparator states.

A problem of this circuit is that in the case that both inputs are equal and there is a delay in the switches the current consumption will increase. As the bias current is divided equally between both input transistors there will be an adaptive current flowing on both loops. To solve this issue two transistors are added, Q13 and Q16, figure 2.6. Considering that the differential input voltage is 0V, equal currents $I_{ref}/2$ will flow through Q1 and Q2. If I_1 is the current flowing in Q19 and Q20:

$$I_1 = \frac{KI_{ref}}{2} - K'I_1 \tag{2.2}$$

$$I_1 = \left(\frac{K}{1+K'}\right)\left(\frac{I_{ref}}{2}\right) \tag{2.3}$$

$$I_{bias} = \frac{I_{ref}}{2}\left(1 + \left(\frac{K}{1+K'}\right) + \left(\frac{K}{1+K'}\right)^2 + ...\right) \tag{2.4}$$

Which is a geometric series, so If $K' + 1$ is larger than K, the series can be reduced to:

$$I_{bias} = \left(\frac{1 + K'}{1 + K' - K} \right) \frac{I_{ref}}{2} \tag{2.5}$$

In this design K and K' were chosen to be 2 and 3 respectively, so $I_{bias} = I_{ref}$. Thus limiting the current consumption when the input signal is near zero.

After the differential pair and the ABCG circuits there are two S-R latches and two logical inverters. As explained before the purpose of the first latch is to hold the result of the comparison and drive the transistor which activate and deactivate the adaptive current. A second latch is used as a buffer, although not strictly necessary, it was seen in simulations that it improved the performance of the comparator. At the output of the second latch the low level is roughly zero but the high level is far from reaching the supply voltage, to solve this issue two logical inverters are connected in series at the output. A complete schematic of the comparator is shown in figure 2.6 and the dimension of the transistors in table 2.2.

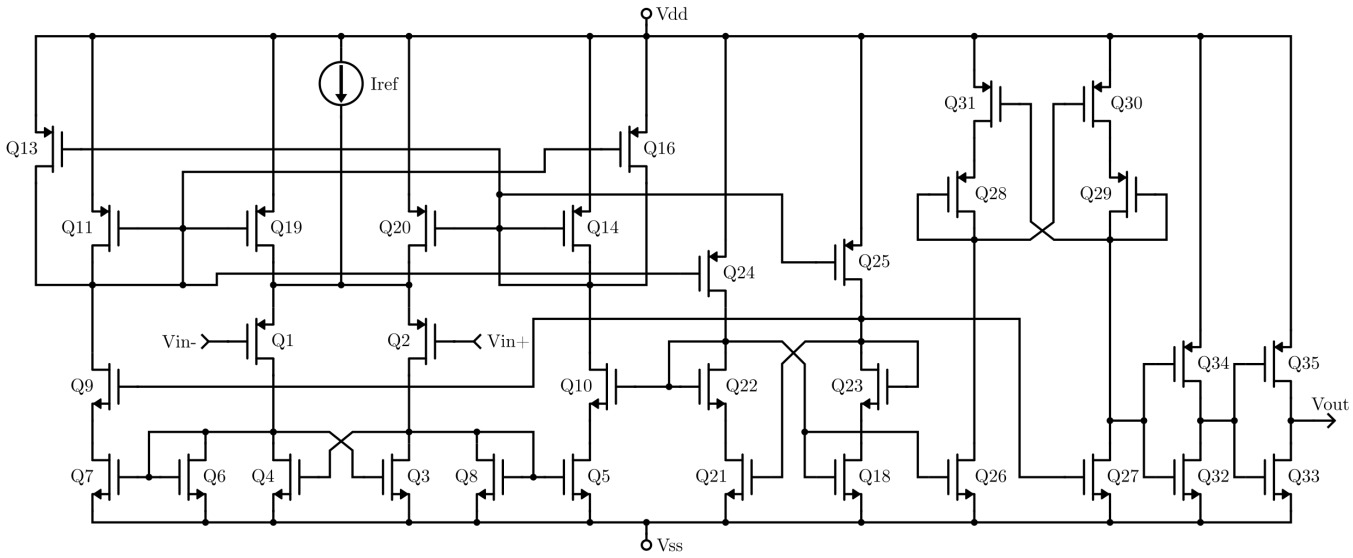


Figure 2.6: Comparator.

Monte Carlo simulations were carried out to assess speed, consumption, offset, supply voltage range and delay. As stated in the introduction, the voltage range selected is from 2V to 3.2V. For each parameter 100 runs were performed, using the libraries provided by the integrated circuit manufacturer which include statistical models.

Transistor	Type	Width(μm)	Length(μm)
Q1, Q2	PMOS	40	4
Q3, Q4, Q6, Q8, Q9, Q10	NMOS	100	10
Q11, Q14, Q19, Q20	PMOS	80	10
Q13, Q16	PMOS	240	10
Q12	PMOS	100	10
Q15	PMOS	198	10
Q24, Q25, Q30, Q31, Q34, Q35	PMOS	4	10
Q22, Q23	NMOS	2	100
Q18, Q21, Q26, Q27, Q32, Q33	NMOS	2	10
Q28, Q29	PMOS	4	100

Table 2.2: Dimensions of the comparator transistors.

2.1.3 Delay

The heart of a healthy person beats no faster than 250 bpm [3] which is a beat every 240ms, with this in mind a delay of up to 5 percent or 12ms could be acceptable. The histogram for the simulated delay is presented in figure 2.7, the maximum value of 3.1ms is well below the critical value proposed.

2.1.4 Offset

The comparator was designed with hysteresis, so the two scenarios must be distinguished: a positive input voltage and a negative input voltage. The largest average offset, of 1.2mV, is for the negative input. The output signal of the filter which also includes the offset of the filter has to be large enough to make accurate detections. A signal amplitude of 10mV at the output of the filter proves satisfactory, furthermore the filter contains an offset trimming functionality which reduces both offsets, explained in 2.2.

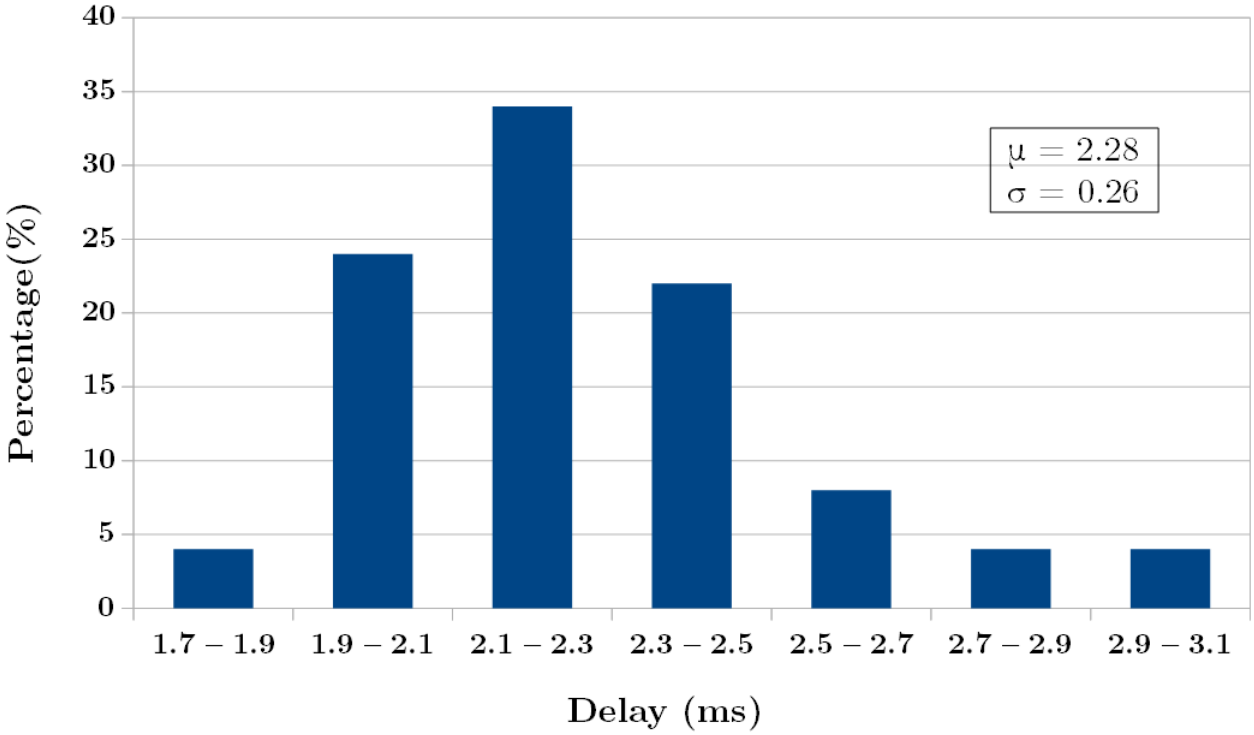


Figure 2.7: Comparator delay.

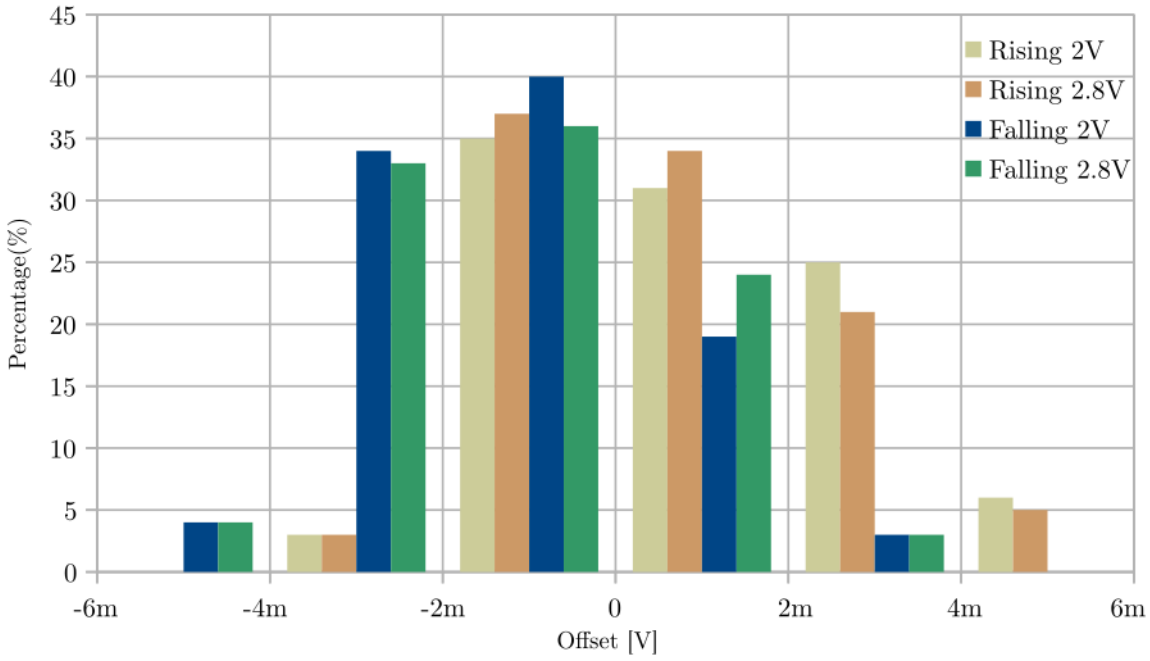


Figure 2.8: Comparator Offset.

Supply voltage(V)	Condition	Average offset(mV)	Standard deviation(mV)
2	Rising	0.86	1.8
2.8	Rising	0.78	1.8
2	Falling	-1.2	1.8
2.8	Falling	-1.2	1.8

Table 2.3: Offset mean and standard deviation.

2.1.5 Current consumption

The current consumption for various supply voltages are shown in figure 2.9 and table 2.4. A Tokyo signal with a period of 300ms was used, this corresponds to a heart rate of 200bpm which is a very demanding scenario, in a real application the average consumption will be lower. One important observation is the large variation of the supply current with different supply voltages, from 31.6nA to 41.5nA. I_{ref} is almost constant as well as the consumption of the latches and inverters, the variation then, is related to the adaptive current.

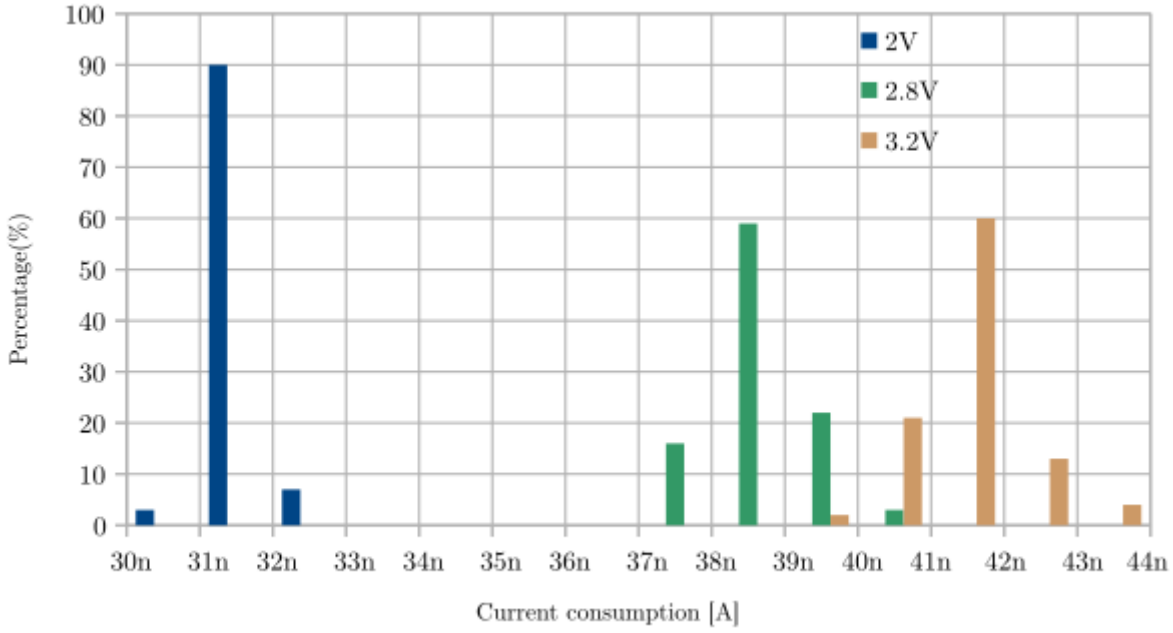


Figure 2.9: Comparator current.

Taking into account the result of the simulations, the characteristics of this comparator

Supply voltage(V)	Average Current(nA)	Standard deviation(nA)
2	31.6	0.28
2.8	38.6	0.59
3.2	41.5	0.70

Table 2.4: Current consumption mean and standard deviation for three supply voltages.

make it suitable for the sensing channel. It has sufficient speed, low offset and consumes less than 50% of the proposed current consumption.

2.2 Filter

According to [20] the cardiac signal has an amplitude between 200μV and 10mV. For signals of 200μV, a gain of at least 50 is needed to achieve an amplitude above 10mV at the output of the filter, as given by the comparators input requirements. Due to the bandpass characteristic some components of the signal will be attenuated by the filter and the amplitude of the signal at the output will be smaller than 10mV as desired. For this reason a larger gain, closer to 100, is sought.

The filter should provide gain of at least 100 and a bandpass characteristic to reject frequencies outside the band of interest. It is also important that it has low offset. Table 2.5 presents the objective design characteristics.

Gain	$\geq 100V/V$
High-pass pole	75Hz
Low-pass pole	250Hz
Offset	$\leq 5mV$

Table 2.5: Filter design objectives.

Several amplifier design techniques were studied to assess their characteristics and viability for this work, the most important were: output transconductance amplifiers (OTA) feedback loop filters, op-amps filters, switched capacitors filters, and translinear filters. A brief description of each type follows.

2.2.1 Types

2.2.1.1 Op-amps filters

This is the most popular type of filter. It is implemented with operational amplifiers and discrete components to set the poles and zeros. Some works have used this type of filter for sensing channels [7] achieving currents as low as 110nA for the filter, without considering the

comparator.

2.2.1.2 Switched Capacitors Filters

Switched Capacitor Filters (SCF) are discrete-time systems which operate in two phases: sampling and amplification. As it is a timed circuit a clock is needed to define the switching phases. SCF are particularly interesting in CMOS technology because high-performance switches can be implemented easily. On the other hand a large portion of the silicon area is devoted to capacitors. The use of transistors as switches also leads to channel charge-injection phenomenon which can affect the capacitor charges and needs to be addressed properly. Some works have achieved a low power consumption using SCF [24], although still far from the proposed consumption for this work.

2.2.1.3 Translinear filters

Although usually applied to bipolar transistors it has been extended to CMOS as well [8], [9] even for all regions of inversion [12]. On the other hand not much publications and applications are available, a sensing channel was designed with this technique achieving a current consumption of 120nA using BJT technology [11]. Bipolar applications were discarded because this work is focused in CMOS technology which is the technology usually employed in pacemakers.

2.2.1.4 OTA feedback loop filters

This type of filters are implemented with OTAs in a feedback loop with other passive components such as capacitors. It can achieve low consumption while still retaining simplicity. The OTAs can be made with standard CMOS transistor. The power consumption can be decreased by decreasing the bias current and making the transistors wider to retain high transconductance. There is also a trade-off between bias current and linear range. This technique has been previously used for the design of sensing channels [20] [16].

It is difficult to compare sensing channels proposed by other authors as no architecture is

similar to the other and different measurements are provided. The most relevant publications are that of: Lentola [24], Silveira [7] and Haddad [11]. Table 2.6 summarizes some of the characteristics of these designs. For this work the last approach, a filter with OTAs, was chosen because of the simplicity and the abundant work available which indicates that it is a feasible way to achieve an extremely low current consumption.

Type	Supply Voltage[V]	Current consumption[A]	Includes comparator?
SCF [24]	2-2.8	1u	Yes
SCF [17]	1	135n	No
Silveira [7]	2-2.8	110n	No
Translinear [11]	2	120n	Yes

Table 2.6: Sensing channels proposed by other authors.

A negative-feedback OTAs loop with a bandpass characteristic was designed. It contains four differential input and single ended output OTAs, and two capacitors as seen in figure 2.10. Equation 2.6 is the transfer function, it has two simple poles and one zero, so the slope of the transfer function is 20dB/dec for the lowpass as well as the highpass characteristic.

$$H(jw) = \frac{gm_1 C_2 jw}{-C_1 C_2 w^2 + gm_3 gm_4 + gm_2 C_2 jw} \tag{2.6}$$

An initial estimation for the transconductances and capacitors using the transfer function provided a starting point for an empirical fine tuning. Many parasitic capacitances, especially that of the current mirrors inside each OTA, proved to have an important effect on the characteristic of the filter. The simulated values are included in table 2.7.

2.2.1.5 OTA

The 4 OTAs used in the filter have the same topology which is presented in figure 2.11. Two input transistors generate input dependent currents which are then subtracted by current mirrors. For low amplitude input signals, the output current is approximated by 2.7.

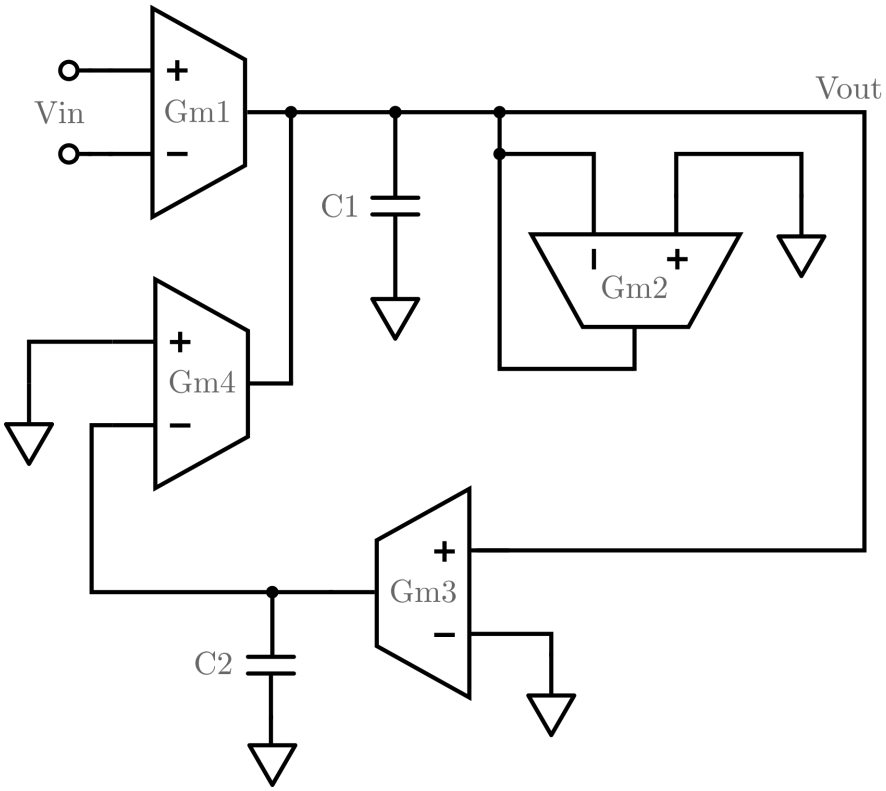


Figure 2.10: Filter schematic.

Parameter	Design	Simulation adjusted	Bias Current(nA)
gm1(max)	315nS	315nS	23
gm2	2nS	10.4nS	0.64
gm3	6nS	8.15nS	0.49
gm4	5nS	42.3nS	2.91
C1	1.7pF	1.7pF	-
C2	350pF	300pF	-

Table 2.7: Filter design objectives.

$$\left.\begin{aligned} I_1 &\approx I_3 \\ I_2 &\approx I_5 \\ I_3 &\approx I_4 \end{aligned}\right\} \Rightarrow I_{out} = I_5 - I_4 \approx I_2 - I_1 \approx \alpha(V_{in+} - V_{in-}) \tag{2.7}$$

The transconductance of the OTA is defined by the bias current I_{ref}, the width to length

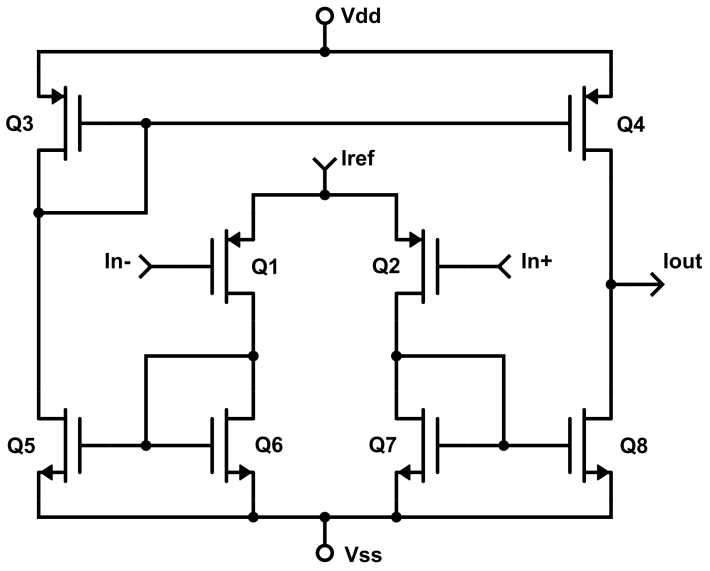


Figure 2.11: Output transconductance amplifier.

ratio of the input transistors and the ratio of the current mirrors. It it is important to work on weak inversion because in this region of operation transistors exhibit the largest transconductance to drain current ratio [13] which is at the same time a good indicator of the inversion level. A rough guide is that, if it is below 5 the transistor is biased in strong inversion and if it is larger than 20 it is biased in weak inversion. Moderate inversion lies in the middle. Figure 2.12 shows the simulated g_m/I_d curve for a PMOS with l=10μ and w=2μ. The curve is theoretically flat for weak inversion but the ratio drops due to leakage currents.

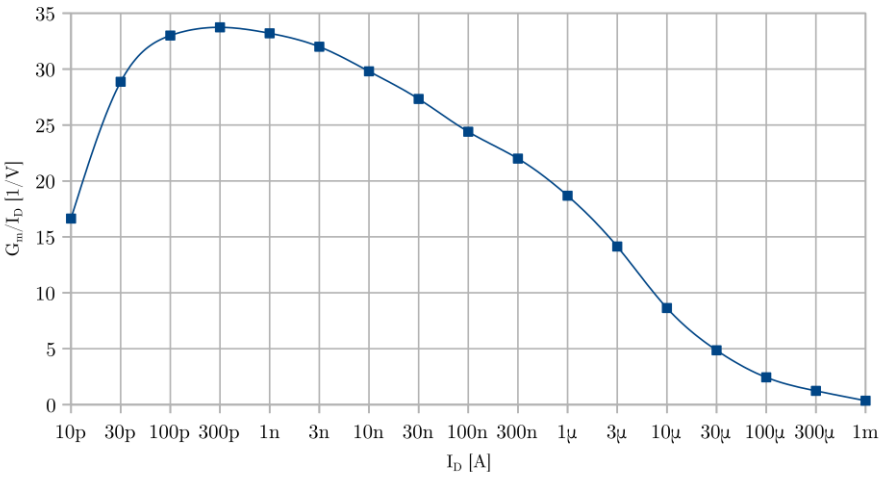


Figure 2.12: Gm to id ratio as a function of id. At low currents, in weak inversion, the maximum ratio is obtained.

The width and length of every transistor in the filter are included in table 2.8. The only transistors that must strictly be biased in weak inversion are the input differential pair of every OTA, this are the transistors that generate most of the gain. The inversion level of the current mirrors is not important, their current consumption does not depend on it. The transconductance to drain current ratio for the input differential pair of every OTA is included in table 2.9. The bias current of the first OTA is variable as explained in the next subsection, still all the differential pairs are biased in weak inversion.

Transistor	Gm	Width(μm)	Length(μm)
Q1, Q2	1	160	32
Q6, Q7	1	40	25
Q5, Q8	1	40	40
Q3, Q4	1	80	80
Q1, Q2	2	100	20
Q6, Q7	2	80	40
Q5, Q8	2	20	40
Q3, Q4	2	20	20
Q1, Q2	3	100	20
Q6, Q7	3	20	35
Q5, Q8	3	20	40
Q3, Q4	3	20	20
Q1, Q2	4	100	20
Q6, Q7, Q5, Q8	4	20	40
Q3, Q4	4	20	20

Table 2.8: Dimensions of the filter transistors.

As low bias currents were chosen, the linear range of every OTA is limited to about 50mV. The most affected are Gm2 and Gm3 because they are biased with only 640pA and 490pA respectively. One of the design criterion is to have a gain of at least 100 and to be able to detect signals with amplitudes as low as 200uV, which translates into a signal of at most 20mV at the output of the filter, this is within the linear limit of the OTAs. On the other end of

OTA	g_m(nS)	I_d(A)	$\frac{g_m}{I_d}(\frac{1}{V})$
Gm1	12.4 - 323	381p - 11.8n	32.5 - 27.4
Gm2	10.7	327p	32.7
Gm3	8.18	251p	32.6
Gm4	46.4	1.49n	31.3

Table 2.9: Inversion level of the input differential pairs.

the spectrum signals of up to 10mV must be amplified as well, this would give a signal with an amplitude of at most 1V at the output if the same gain of 100 remains unchanged. This exceeds the linear range available, a possible solution is to adjust the gain in accordance with the amplitude of the input signal. Taking a look at the transfer function of the filter the transconductance of the first OTA, Gm1, has no effect on the poles placement but only on the overall gain. Adjusting the bias current of this OTA is ideal to reduce gain without affecting the transfer characteristic and keeping the input signal within the acceptable linear range.

2.2.1.6 Gain setting

A simple digitally controlled current mirror is implemented to bias Gm1. It is driven by a 5 bit word and can provide bias currents in the range of 1.25nA to 38.75nA with a step of 1.25nA. The changes in gain are equidistant for consecutive digital words. The schematic can be seen in figure 2.13 and the dimension of the transistors in table 2.10.

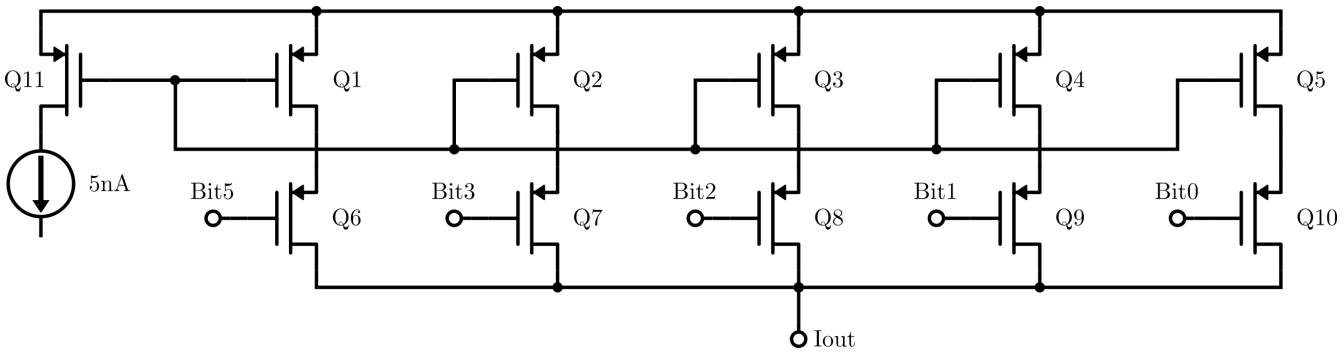


Figure 2.13: Gain control circuit.

The magnitude of the transfer function of the filter is shown in figure 2.14 for several gain

Name	Width(μm)	Length(μm)
Q6, Q7, Q8, Q9, Q10	10	10
Q1	240	10
Q2	120	10
Q3	60	10
Q4	32	10
Q5	17	10
Q11	200	20

Table 2.10: Transistors dimensions.

settings, including the largest and the smallest. The poles and zeros placement is not affected by the variations of Gm1 as predicted.

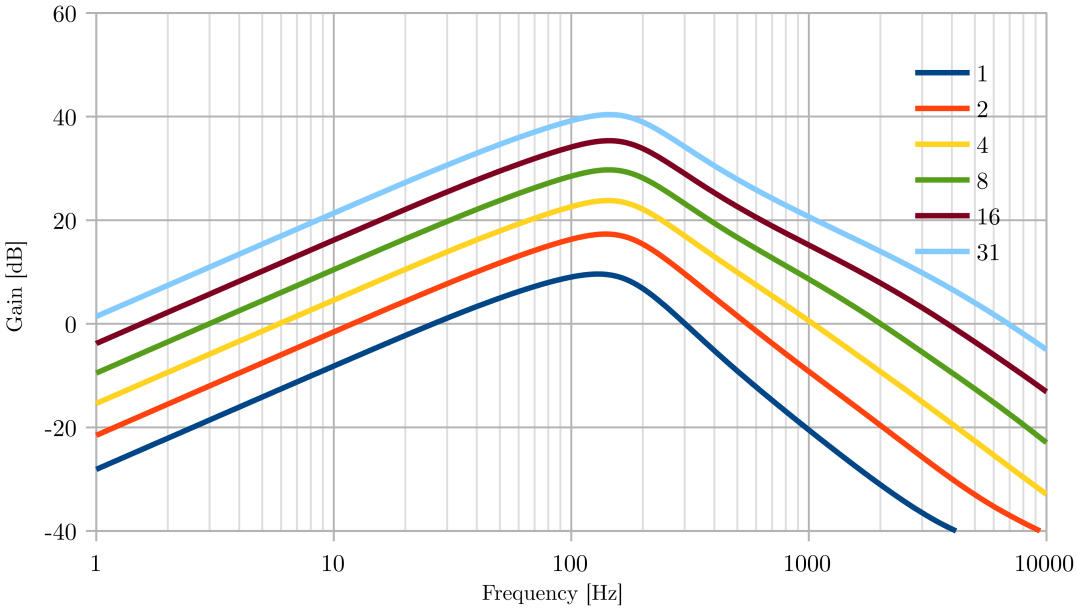


Figure 2.14: Filter magnitude response for several gain settings.

It is also important to study the evolution of the filter response for the whole supply voltage range, figure 2.15 presents the magnitude of the filter for supply voltages starting at 2V up to 3.2V with a step of 0.1V and the gain control set to 16 (medium gain), the filter performance is practically unaffected.

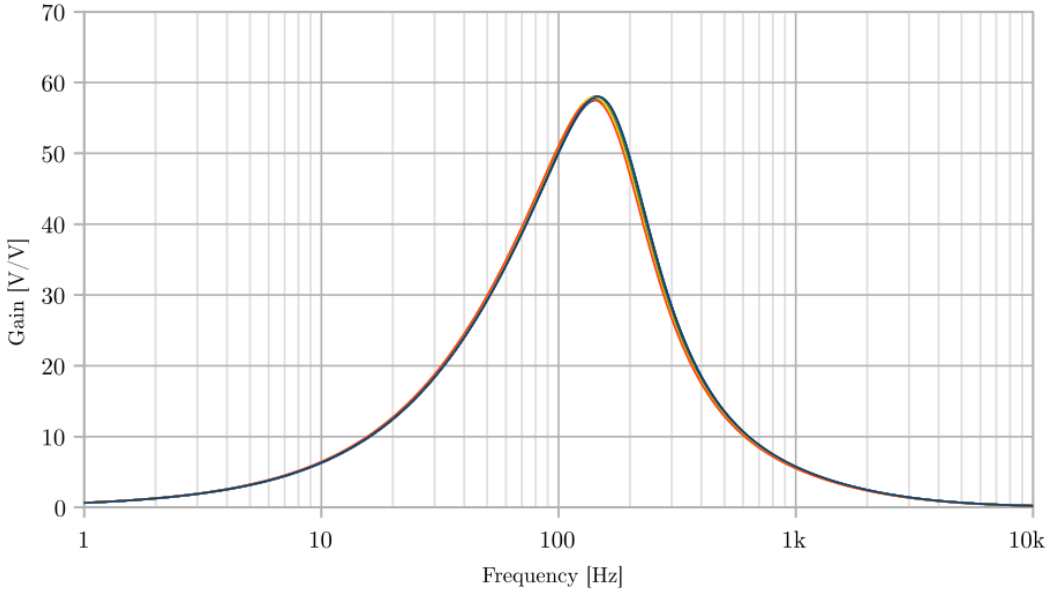


Figure 2.15: Filter magnitude response for several supply voltages. The measurements are taken with the control bits set 10000 (16), which is the medium gain.

2.2.2 Offset

If an amplifier inputs are at the same voltage the output voltage should be zero, although this is not usually the case. Random phenomena in the manufacturing process and design compromises generate a small voltage at the output which is called offset. A histogram of the offset of the filter is shown in figure 2.16. For this measurements the highest gain was used and a 2.8V supply voltage. 100 simulations considering the process parameter deviations were done.

Besides the manufacturing uncertainties and tolerances, the asymmetrical characteristics of the OTA in figure 2.11 generates offset. The average offset for the complete filter is close to 1mV at the output but it has a considerable deviation, figure 2.16. The highest probable offset added to that of the comparator can be comparable to the amplitude of the cardiac signal, consequently an offset trimming mechanism must be employed. One easy way to add or subtract an offset voltage to this filter is to include a variable DC current source in parallel with capacitor C2. This can be implemented by two current sources, one which feeds current into the node and and another which feeds current out of the node, the current difference generates the offset voltage. The filter with the offset-tuning mechanism is presented in figure 2.17.

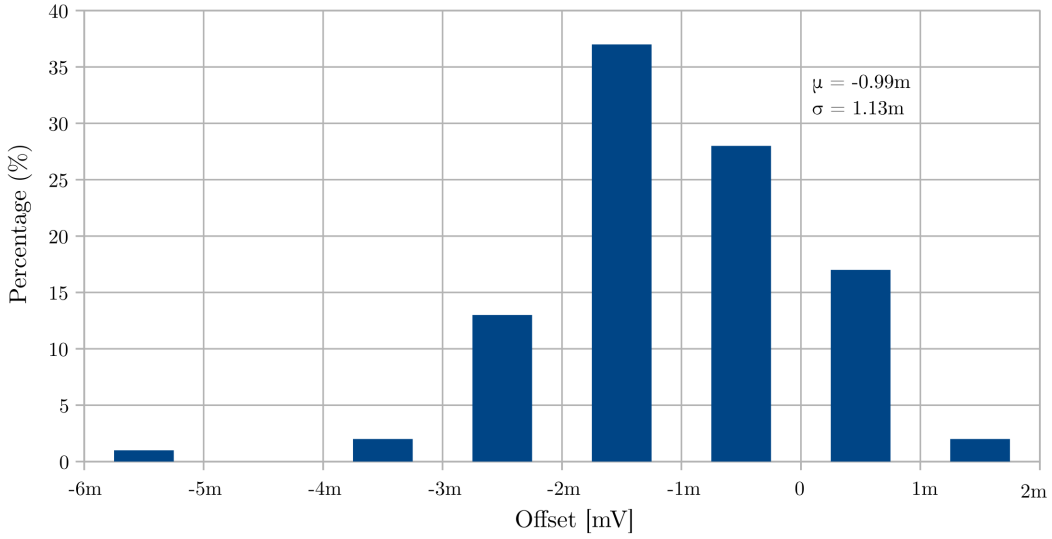


Figure 2.16: Filter offset distribution.

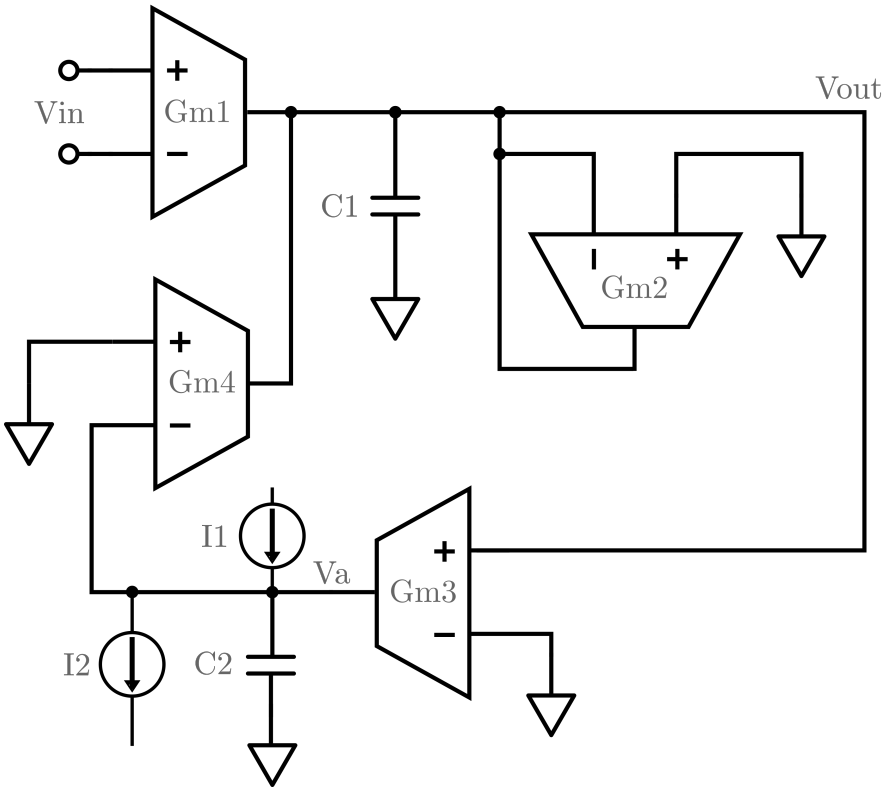


Figure 2.17: Filter with offset control.

I_1 provides a fixed current of 87pA while I_2 is digitally controlled variable current source which can provide currents from 10 (due to leakage currents) to 166pA in steps of 4.9pA. The trimming current is in the range of -79pA to 77pA. When there is no input signal the transfer function, taking the trimming current as the input, is:

$$Z(0) = \frac{V_o}{I_2 - 1_1} = \frac{1}{gm_3} \tag{2.8}$$

With the measured gm_3 of 8.18nS the output voltage variation is between -9.41mV to 9.66mV with a step of 596μV. The offset trimming circuit is driven by a digital logic explained in section 2.4.

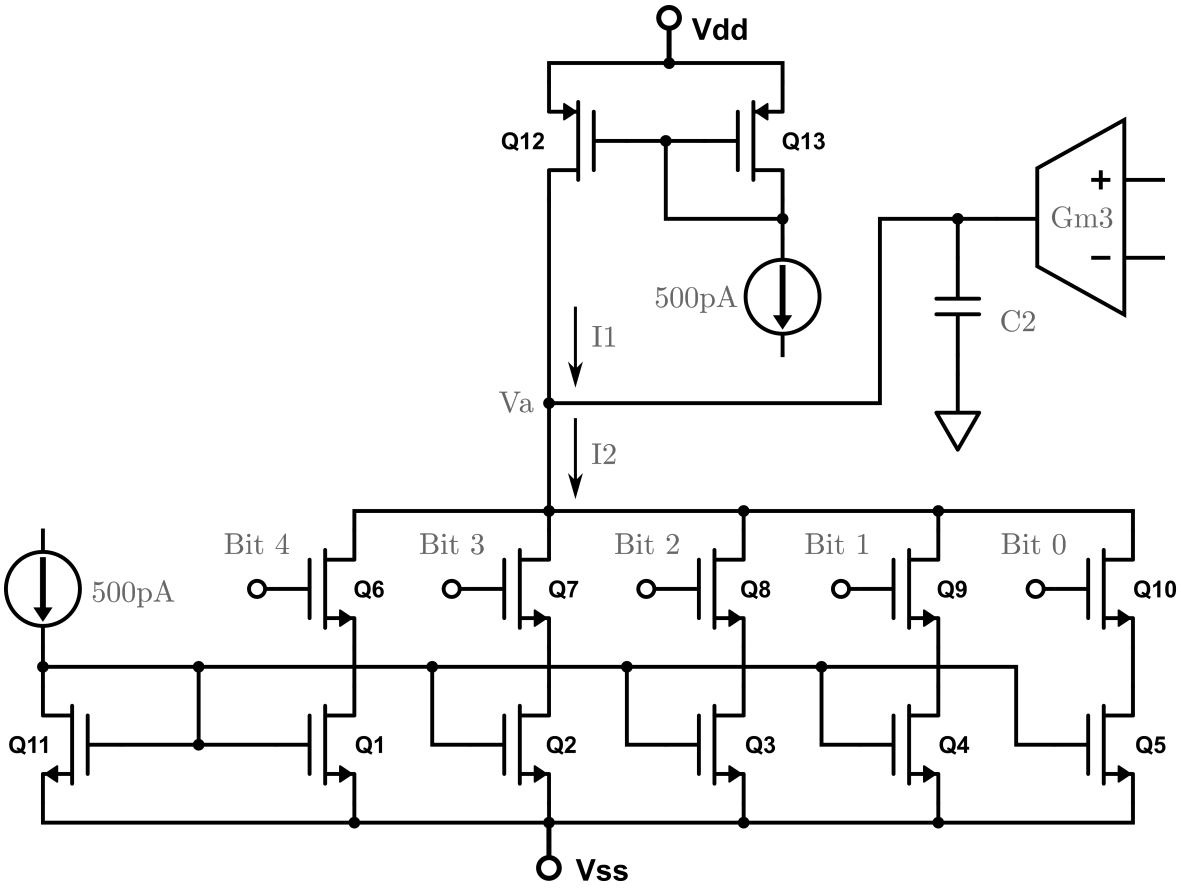


Figure 2.18: Schematic of the offset correction mechanism.

I_1 is implemented with a simple current mirror, taking a reference of 500pA and a division ratio of 6. I_2 is made of a set of 5 digitally controlled current mirrors in parallel, figure 2.18. The dimensions of the transistors are included in table 2.11.

2.2.3 Stability

To study the stability of the circuit Montecarlo simulation were performed to measure the phase margin. The average is 49 degrees and never goes below 47 degrees. The phase margin

Name	Width(μm)	Length(μm)
Q6, Q7, Q8, Q9, Q10	10	10
Q1	80	10
Q2	42	10
Q3	22	10
Q4	12	10
Q5	7	10
Q11	500	10

Table 2.11: Transistors dimensions.

showed little variation with different gain settings, as expected because Gm1 does not play a role in stability.

2.2.4 Noise

Spontaneous fluctuations in the current and voltage due to the discrete characteristic of electronic charge generate electronic noise [13]. Noise limits the signal-to-noise ratio of an amplifier. Two types of noise that affect CMOS devices are: thermal noise and flicker noise. Thermal noise is generated by the random motion of electrons in the channel of transistors and its power spectral density (PSD) is constant for all frequencies, theoretically. That its why it is also known as white noise. Equation 2.9 presents a model for thermal noise, where T is the temperature, k the Boltzmann constant and n is a parameter of the transistor modeling.

$$S_{th} = 2nkTg_m \tag{2.9}$$

If a transistor is biased in weak inversion, the transconductance to drain current ratio approaches 2.10, n can be obtained as the left hand side is obtained from simulations and ϕ_t is the thermal voltage given by 2.11, where k is the Boltzmann constant.

$$\frac{g_m}{I_d} = \frac{1}{n \cdot \phi_t} \tag{2.10}$$

$$\phi_t = \frac{k \cdot T}{q} \tag{2.11}$$

Flicker noise appears in the interface between the silicon substrate and the gate oxide, were new energy states appear. As charge carriers move at the interface, some are trapped to be later released by these energy states generating flicker noise in the drain[14]. Its PSD is proportional to the inverse of the frequency. Several models exists, one of the simplest is the Spice 2 model given by equation 2.12 [25]. The constants are supplied by the integrated circuit manufacturer and their values for the XC-06 process are included in table 2.12.

$$S_f = \frac{K_F \cdot I_{ds}^{af}}{C_{ox} \cdot L_{eff}^2 \cdot f^{ef}} \tag{2.12}$$

Parameter	PMOS	NMOS
K_F	$5 \cdot 10^{-30}$	$3 \cdot 10^{-28}$
af	1	
ef	1	1.2
C_{ox}	$2.76 \cdot 10^{-15}$	

Table 2.12: Noise constants.

For the estimation of the input noise, the lowest bias current in Gm1 is used, as this is the worst case. The thermal and flicker noise of every OTA are calculated at its output, table 2.13. To estimate the total noise power at the output of the filter, the transfer function from each noise source to the output of the filter must be obtained firstly. G_{m1}, G_{m2} and G_{m2} feed their noise current to the same node, so the transfer function needs to be calculated only once 2.14. Equation 2.15 is the transfer function for G_{m3}. To obtain the PSD at the output of the filter, the relation 2.13 valid for linear time-invariant (LTI) systems, is used.

$$S_y(f) = |H(f)|^2 \cdot S_x(f) \tag{2.13}$$

Once all the noise sources are at the output, an integration over the whole frequency range is performed to obtain the noise power at the output. Once again, applying 2.13, the output

noise power is divided by the square of the maximum gain of the filter to obtain the noise power at the input. The square root of this quantity is the RMS noise at the input.

OTA	Thermal noise [V^2/Hz]	Flicker noise[V^2]
G_{m1}	$4.64 \cdot 10^{-28}$	$2.10 \cdot 10^{-15}$
G_{m1}	$1.28 \cdot 10^{-28}$	$1.20 \cdot 10^{-15}$
G_{m1}	$4.83 \cdot 10^{-28}$	$4.78 \cdot 10^{-15}$
G_{m1}	$3.25 \cdot 10^{-27}$	$3.37 \cdot 10^{-14}$

Table 2.13: OTAs noise.

$$H_1 = \frac{V_o}{I_n} = \frac{-G_{m4}}{C_1C_2s^2 + G_{m2}C_2s + G_{m3}G_{m4}} \tag{2.14}$$

$$H_2 = \frac{V_o}{I_n} = \frac{C_2s}{C_1C_2s^2 + G_{m2}C_2s + G_{m3}G_{m4}} \tag{2.15}$$

The total noise power at the input is:

$$V_{nin}^2 = \int_0^\infty \frac{\Big(S_{th3} + S_{f3}\Big)|H_2(f)|^2 + \sum_{i=1,2,4}\Big(\Big(S_{thi} + S_{fi}\Big)|H_1(f)|^2\Big)}{G_{max}^2} df = 1.29 \cdot 10^{-12}V^2 \tag{2.16}$$

$$V_{ninRMS} = 1.14\mu V \tag{2.17}$$

The noise at the input is almost two orders of magnitude smaller than the minimum input signal, $200\mu V$ this probes the circuit is suitable for the application, from the perspective of noise.

2.2.5 Current consumption

The current consumption of the filter is simulated for three supply voltages: 2V, 2.8V and 3.2V. For each voltage a Monte Carlo simulation is performed with 100 runs including the random parameter variations of the manufacturing process. The gain is set to maximum and

the input signal is a Tokyo with an amplitude of 200μV and a frequency of 3.33Hz corresponding to a heart rate of 200bpm. This is above the most current demanding scenario. Figure 2.19 presents a histogram for each simulation, the average and standard deviation are shown in table 2.14. When powered with the highest voltage the circuit draws around 2% more current than with the lowest voltage, so the supply voltage has little impact in the current consumption of the filter.

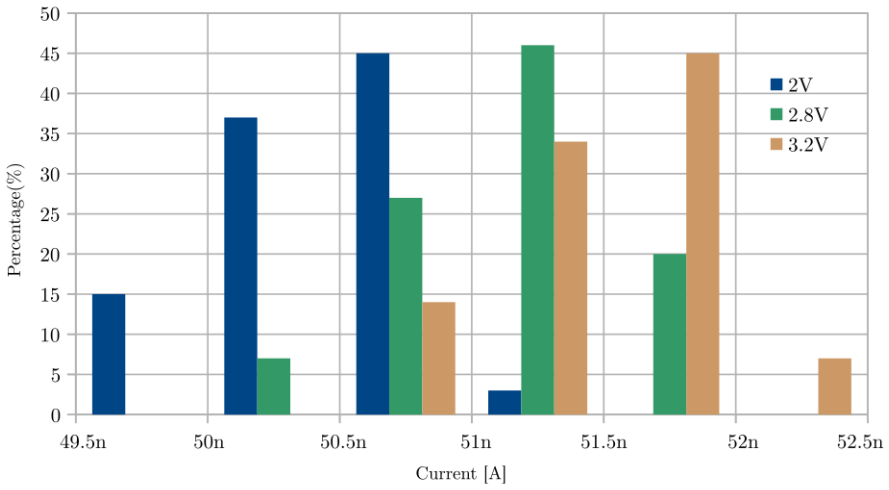


Figure 2.19: Filter current consumption distribution.

Supply voltage(V)	Average current(nA)	Standard deviation(nA)
2	50.4	0.38
2.8	51.2	0.39
3.2	51.5	0.39

Table 2.14: Current consumption.

To close this section it can be said that the use a of Gm-C filter was the right choice, it provides high gain with minimal current and insignificant noise. It includes a simple interface to set the gain and also offset trimming capability.

2.3 Current sources

The filter needs 5 current sources to operate, 3 to bias Gm2, Gm3, Gm4 and 2 to bias the offset trimming circuit. Gm1 biasing is the gain control circuit. The comparator also needs a current source. These 6 sources are provided by a current mirror which takes an input of 5nA and generates the required currents. Table 2.15 shows the devices current requirements and the sizes of the transistor of the current mirror that generate each.

Device	Bias current(nA)	Width(μm)	Length(μm)
Mirror reference	5	100	10
Gm2	0.64	15	10
Gm3	0.5	12	10
Gm4	2.9	60	10
Offset trimming 1	0.5	12	10
Offset trimming 2	0.5	12	10
Comparator	10	198	10

Table 2.15: Current mirrors.

2.4 Digital Circuit

The proposed Filter and Comparator architecture require a digital circuit to carry out the offset trimming procedure and to hold the result in memory. The trimming drives the offset setting but not the gain of the first OTA, the latter must be performed by the physician after the pacemaker has been implanted. The offset trimming circuit has three inputs, the reset signal, the digital clock and the output of the comparator. The general diagram of the sensing channel is presented in figure 2.20 and the schematic of the digital circuit in figure 2.21.

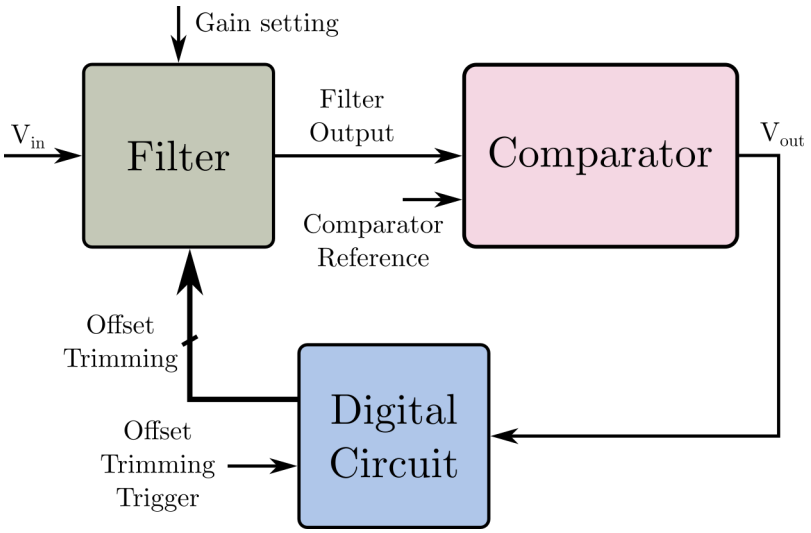


Figure 2.20: Digital circuit diagram.

The idea of the trimming procedure is to begin with the offset at its maximum value and decrease it, step by step, until the comparator switches its output. At this point the current offset setting counteracts both the offset of the filter and the offset of the comparator. After this value is found, it is increased by 1.2mV to reject noise, stored in a set of latches and normal operation resumes.

As depicted in figure 2.21, the circuit includes one 3-bit counter, one 5-bit counter and some other logical components. The clock input of the 5-bit counter is the most significant bit of the 3-bit counter. On a rising edge of the reset signal both inputs of the filter are connected to Vref through Q1 and Q2, the two counters are cleared and also the auxiliary flip-flop U9. In this configuration the offset at the output of the filter is 9.66mV because all of the transistor in the trimming circuit are turned on, Q6 through Q10 in figure 2.21. The comparator output

is 0.

Every time the 3 bit counter output is equal to 111 a pulse is generated by U18 but the output of U19 will still be low as long as the comparator output remains in 0. The 5 bit counter will continue running. When the comparators output switches to 1 the current offset setting compensates the filter and comparator offset.

Now flip-flop U9 will be set and U11 and U19 disabled, as a result the counters will stop, holding the actual value. This offset setting can be problematic as any noise or interference could make the comparator produce a false detection. To avoid this situation the 5-bit counter is increased by two after comparators output turns high. With this modification, the comparator will make a detection when the filter output is larger than 1.2mV, this value was found experimentally. Finally Q1 and Q2 are turned off so the input signal is unaffected.

U12, U13, U14 are used to generate the pulse at U15 outputs when the 3 bit counter reaches seven. U16, U17 and U18 are needed to remove spurious spikes.

The circuit was tested with clock periods of 10ms and below, a greater period is preferred because it helps to diminish the effect of the comparator delay in the trimming process. The maximum time a trimming can take is 256 clock cycles. This is not a periodic offset reduction technique like auto-zero which is usually performed many times per second, it can be done sporadically or every time the physician requires it. Although not a power hungry process, trimming inhibits sensing.

The digital cells are taken from the library provided by the manufacturer and the asymmetrical inverters U16 and U17 are custom made, the dimension of the transistors can be seen in table 2.16.

The presented circuit is validated in section 2.5. With few logic gates and flip-flops the offset trimming logic is performed successfully. As trimming is rarely performed the power consumption is mostly static and it is extremely low.

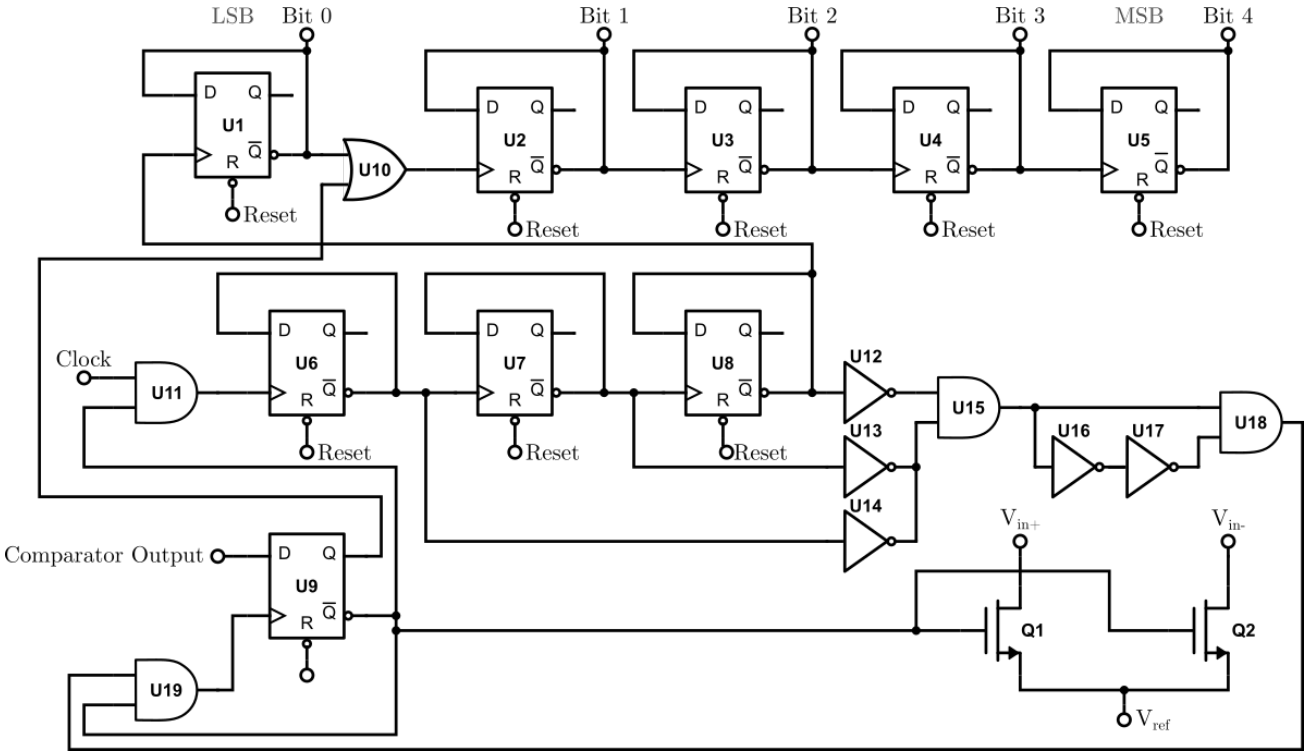


Figure 2.21: Digital Circuit.

Transistor	Type	Width(μm)	Length(μm)
U16	NMOS	2	40
U16	PMOS	10	2
U17	NMOS	40	2
U17	PMOS	2	10
Q1, Q2	NMOS	4	10

Table 2.16: Dimensions of the inverters transistors and input switches.

2.5 Sensing channel simulations

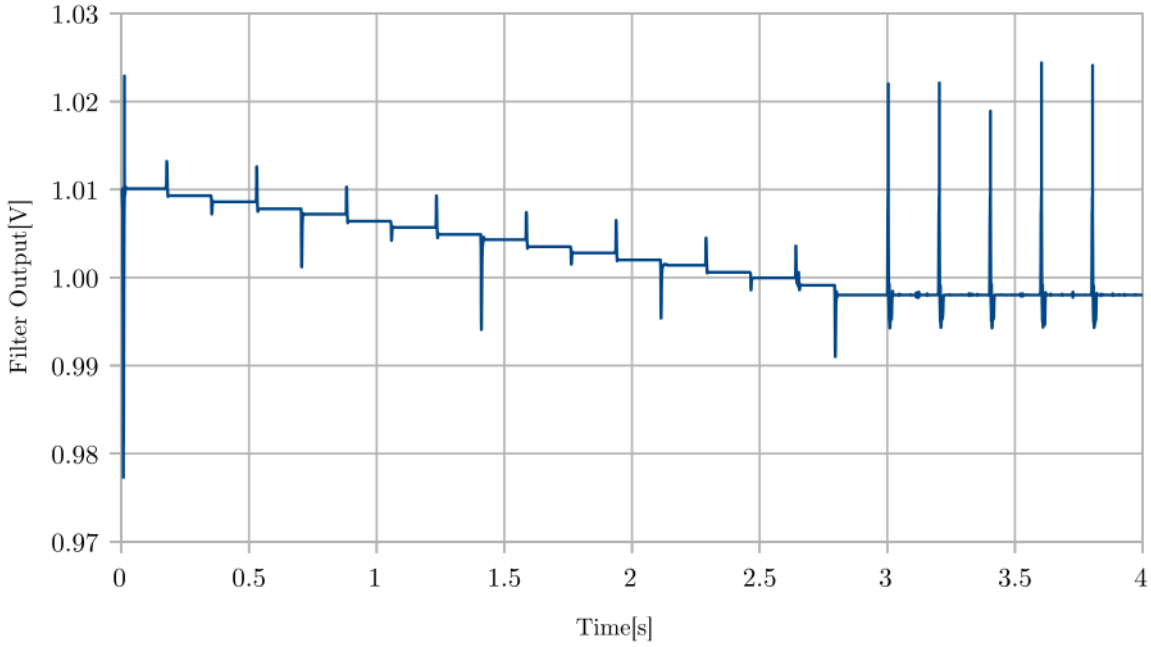
Figure 2.22 a and b presents the signal at the output of the filter and at the output of the comparator respectively. The first stage corresponds to the trimming phase and after trimming finishes a Tokyo test signal with an amplitude of 200μV is applied, the pulses frequency is 5Hz. The output of the filter can be seen in more detail in 2.23. The supply voltage is 2.8V and the reference voltage 1V. All the simulations were performed with Tanner Tools T-Spice v13.0.

The simulation of a trimming and detection cycle takes several seconds and demands processing power and memory, for this reason not more than 5 Montecarlo simulations could be performed simultaneously with up to 10 pulses each. Not a single detection was missed in the simulations performed.

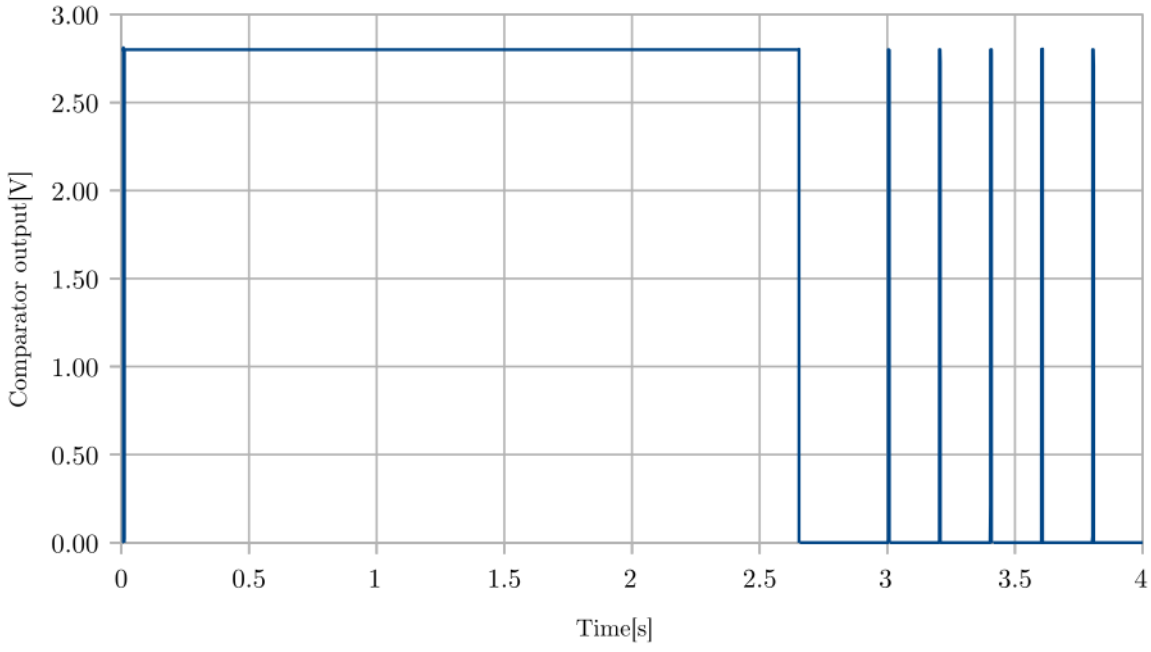
2.5.1 Current consumption

Two cases of current consumption were studied, the first is the most demanding, a Tokyo signal with a period of 300ms and the gain set to maximum. For this scenario the current consumption was measured for a range of supply voltages starting at 2V up to 3.2V in increments of 100mV. As expected by the comparators performance the current consumption depends on the supply voltage, the current consumption as a function of the supply voltage for the whole circuit is shown in figure 2.24.

The second measurement is the static consumption, with no input signal applied. For a supply voltage of 2.8V it is 76nA and is roughly the same for the whole supply range. Most of the current is consumed by the filter and the comparator, the digital circuit draws only 600pA.



(a)



(b)

Figure 2.22: (a) Filter output (b) Comparator output

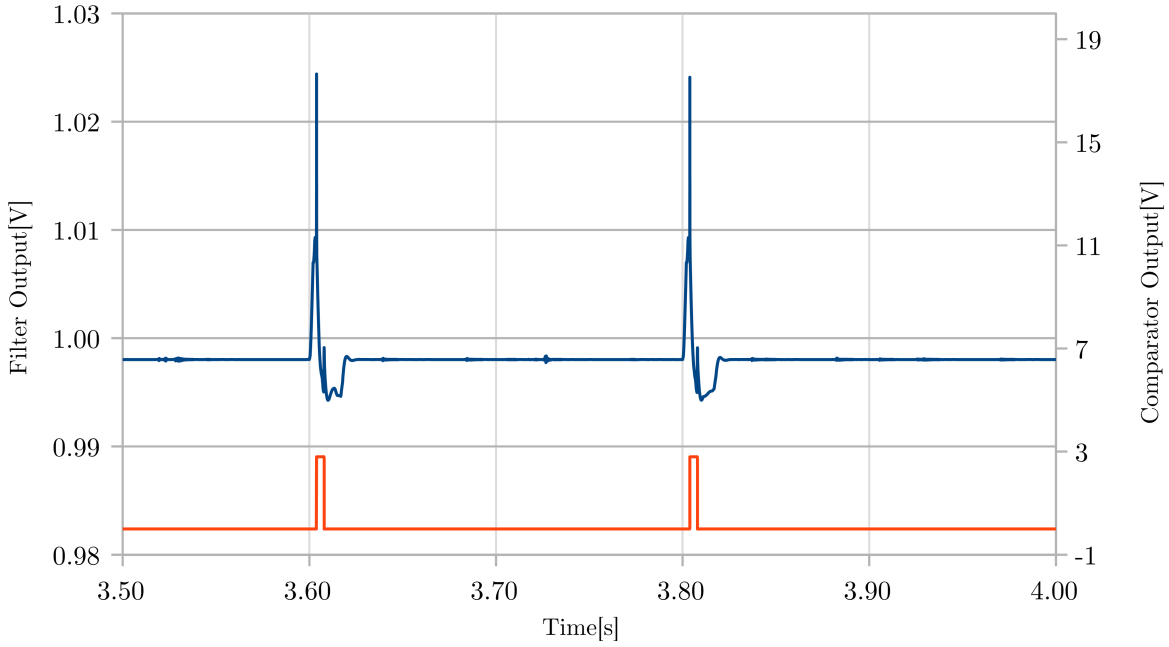


Figure 2.23: Filter output with a train of Tokyo pulses at the input.

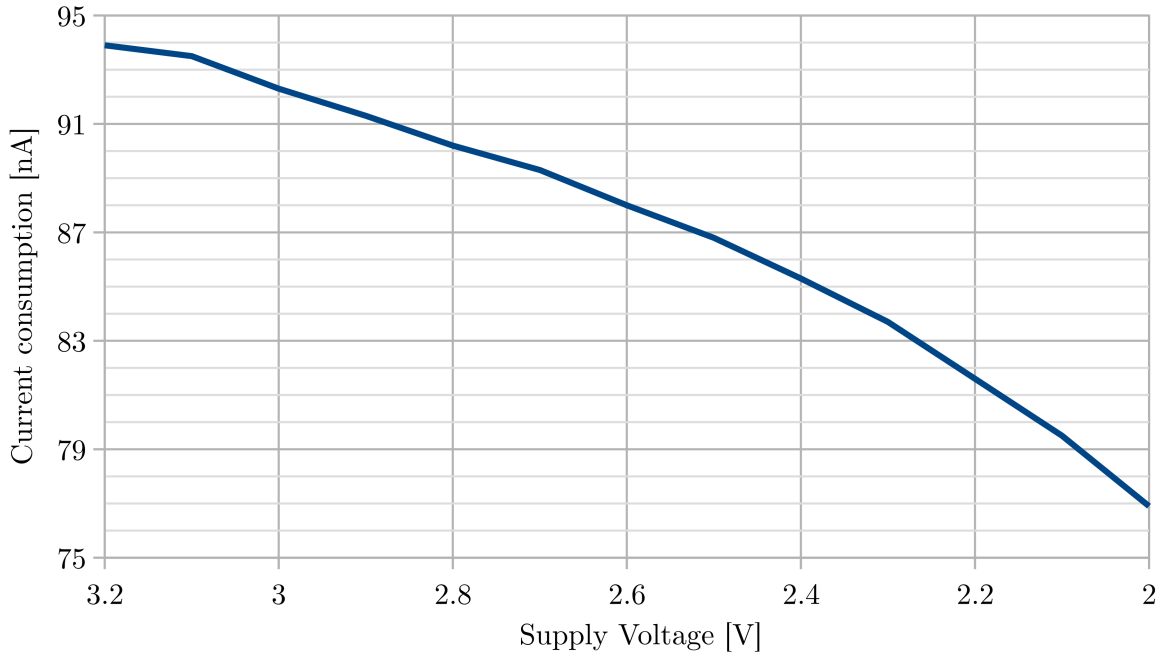


Figure 2.24: Total current consumption as a function of supply voltage.

Chapter 3

Layout

This chapter is dedicated to the layout of the circuit. Each sub circuit is presented and the different layout techniques explained. The dimensions without pads can be seen in table 3.1 and the layout of the whole circuit in figure 3.1. The layout was done with Tanner Tools L-Edit v13.0.

Area	0.79 mm^2
Width	774um
Length	1021um

Table 3.1: Layout dimensions.

The four OTAs have the same structure, they only differ on the transistor sizes, the layout of Gm_1 is presented in more detail in figure 3.2, the upper block corresponds to the differentail pair, followed by the two NMOS current mirrors and the PMOS current mirror at the bottom.

To minimize mismatch and optimize area usage, large transistors have been made of parallel and/or series connections of smaller ones. Transistors that form a pair, like those found in current mirrors and differential pair are split in two rows of smaller ones and scrambled.

As seen in figure 3.3, the transistor connection has been designed to obtain currents in opposite directions for the same transistor, as to counteract the effects of gradients in the manufacturing process. To diminish border effects, dummy transistors are placed on every end,

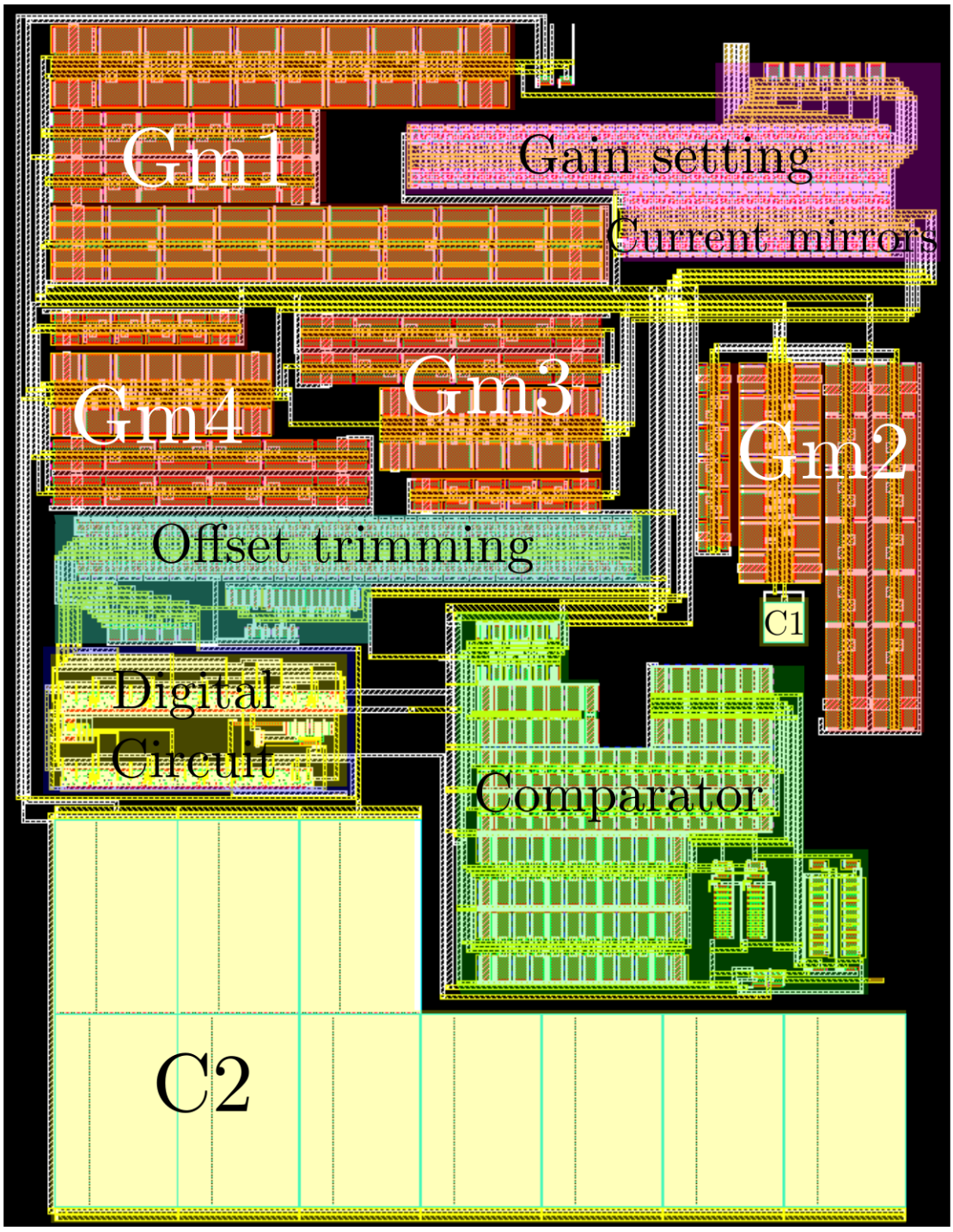


Figure 3.1: Circuit layout.

this was done for every transistor that handles analog signals in the circuit, not for the case of digital switches. Dummy transistors add no electrical function, it serves only the manufacturing process to achieve even transistors.

The layout of the offset trimming circuit, the current mirrors that generate the bias currents

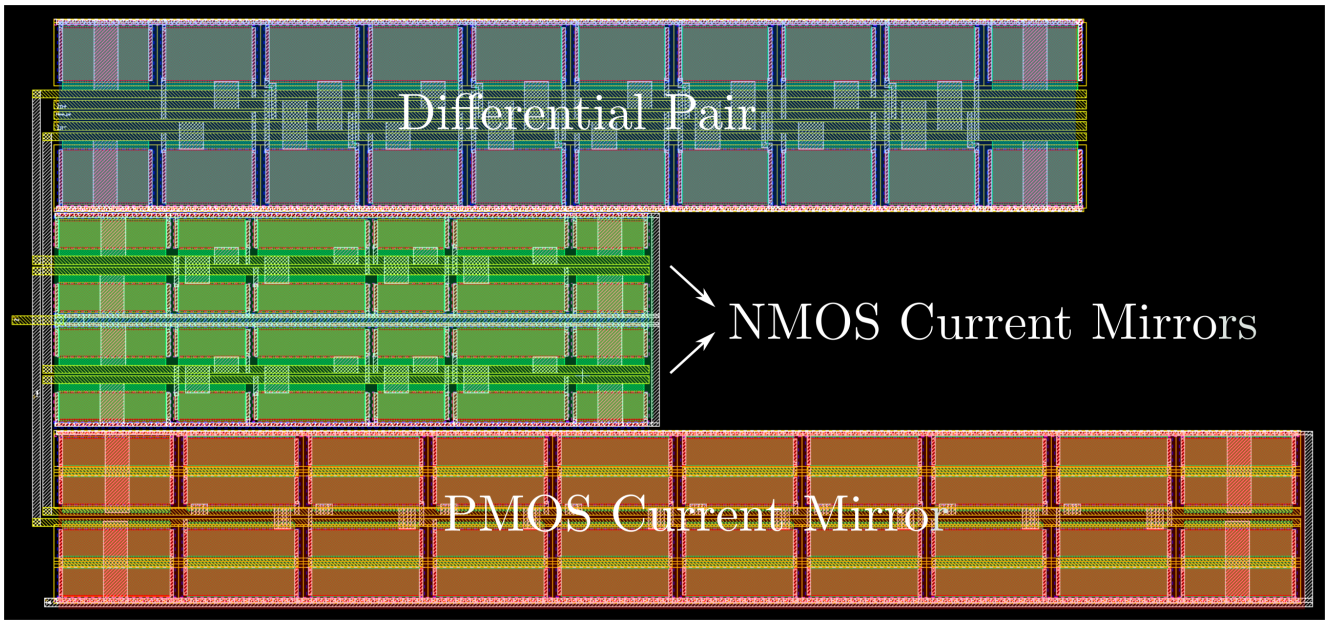


Figure 3.2: Layout of an OTA.

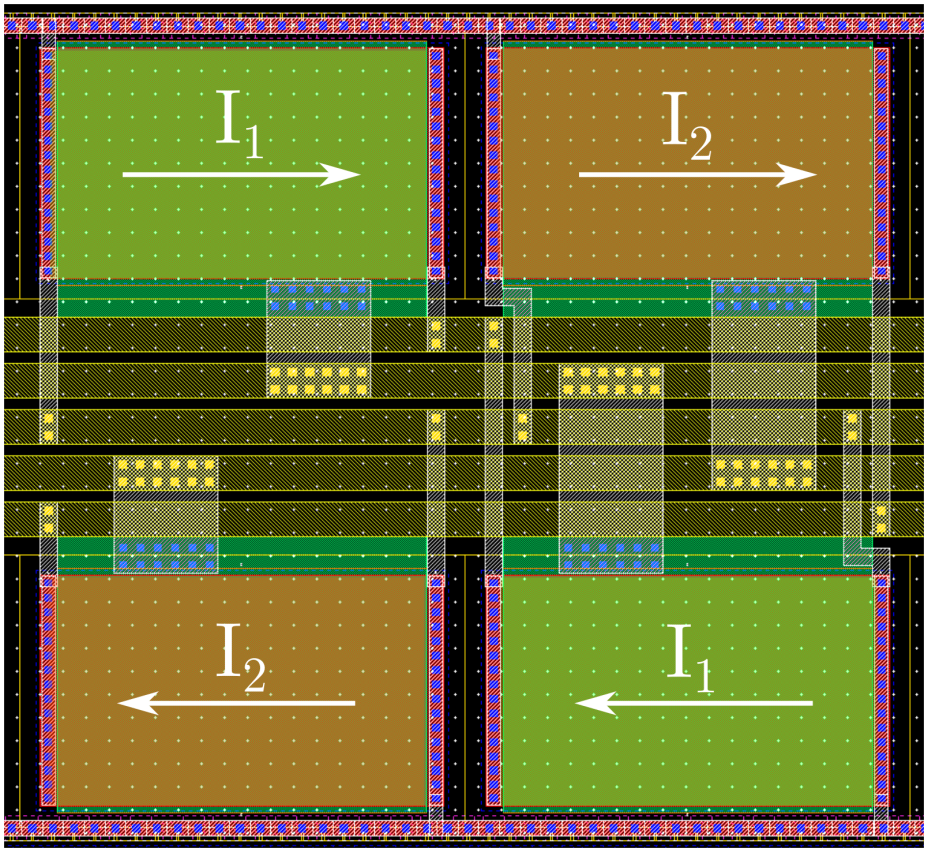


Figure 3.3: Transistor design.

for all the subcircuits and the gain control are mostly made of current mirrors. These current mirrors are implemented with transistor with different width to length ratio with the gates

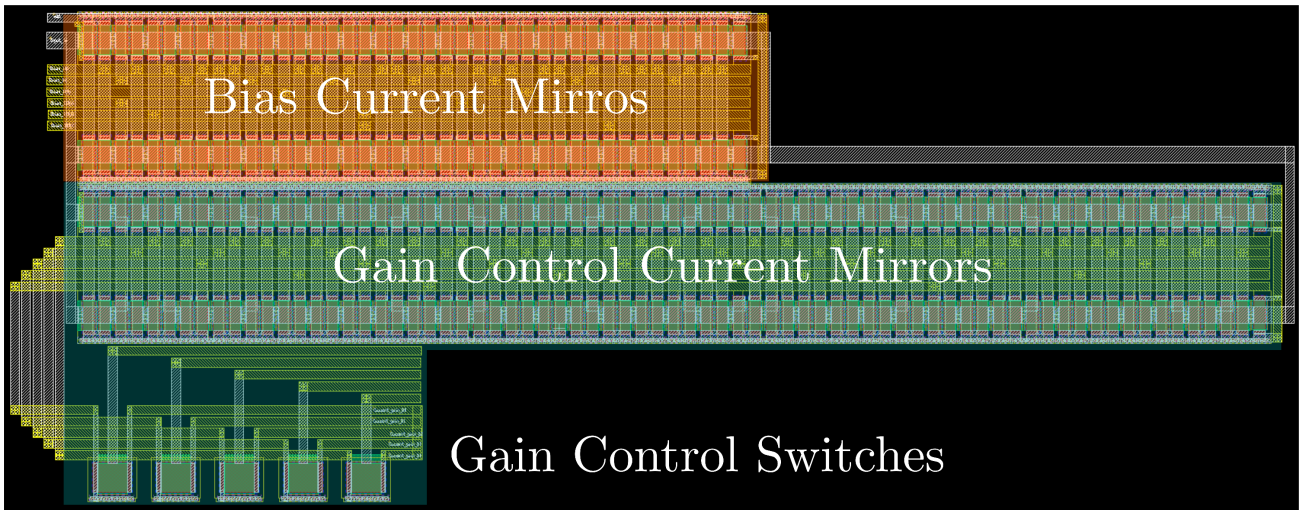


Figure 3.4: Gain control layout.

connected to the same node. It is easier to place transistors vertically side by side so the gate is common, figures 3.5, 3.6, 2.7 and routing is more compact and neat. Transistors are alternated in a way that each of them is uniformly distributed in the whole current mirror. Dummy transistors are added to each end as well.

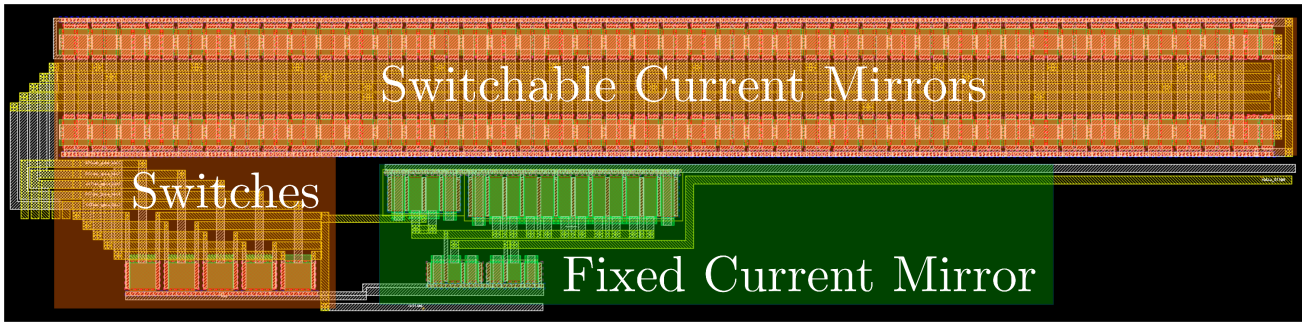


Figure 3.5: Offset control layout.

Figure 3.6 is the comparator layout, it contains several current mirrors and a differential pair in which the same techniques mentioned above were employed. Most of the area is used by the current mirrors, the latches and logical inverters can be seen at the bottom right.

Even though XC-06 offers three metal layers, only two were needed. The third layer could prove useful when integrating the sensing channel into a complete pacemaker chip. The positive supply voltage V_{dd}, the reference voltage V_{ref} and ground V_{ss} are distributed using thick metal lines, at least 3μm wide, usually 6μm or 9μm.

The plates of capacitors C1 and C2 are made of the two polysilicon layers available. C2

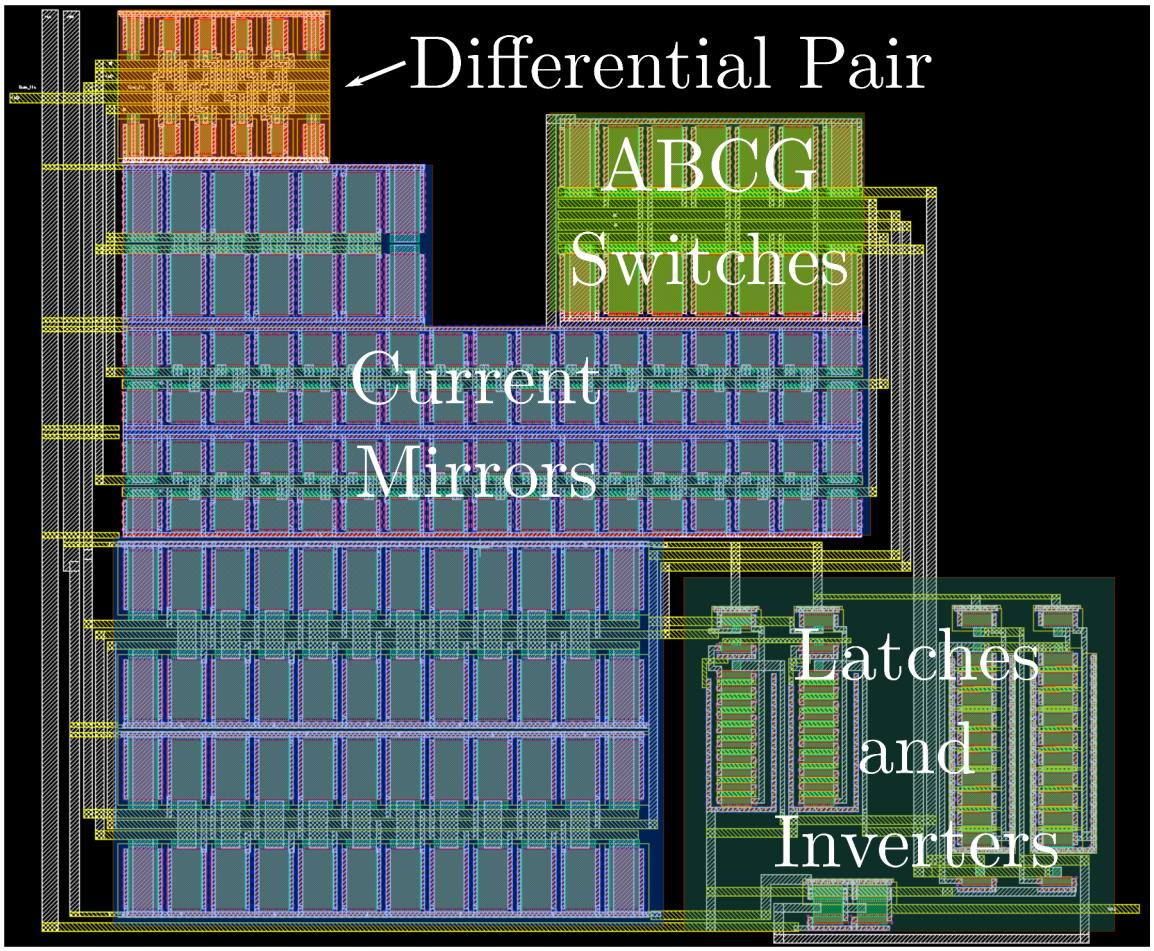


Figure 3.6: Comparator layout.

requires the largest area, square millimeter $0.16mm^2$.

Chapter 4

Conclusions

9

4.1 Conclusions

A cardiac sensing channel to be integrated in pacemakers with a current consumption of 90.2nA has been designed and simulated, making it the sensing channel with the smallest current consumption published up to date as seen in table 4.1. The circuit complies with the requirements of [2] and is designed in 0.6μm high voltage CMOS process. This technology allows the full integration of a pacemaker as the stimulation stage requires high voltage transistors. It is designed to be powered by Li-Io battery, usually employed in implantable devices, with a nominal voltage of 2.8V.

Several simulation were carried out to asses the performance of the circuit, including: bandwidth, offset, current consumption and delay measurements. The manufacturing process deviations were also included in the Montecarlo simulations.

This sensing channel does not protect against electrodes reversal. If this issue is to be addressed, another comparator with the inputs reversed could be included, this would bring the total current consumption to around 130nA which is still not far from the objective.

The layout of the integrated circuit is also included, its area is $0.79mm^2$. Various techniques to reduce mismatch and the effect of gradients have been used. If a second comparator is added some additional area will be needed, around $0.16mm^2$.

Finally, the designed sensing channel will be manufactured and tested to validate the simulated results and perform an in-depth study of the detection failure rate.

Type	Filter[nA]	Comparator[nA]	Total[nA]	Input signal
Lentola et al. [24]	600	400	1000	Unknown
Chiang et al. [17]	135	-	-	Unknown
Silveira et al.[7]	90	20	110	None
Haddad et al. [11]	-	-	120	None
This Work	51.6	38.6	90.2	340ms period

Table 4.1: Sensing channels current consumption.

4.2 Future Work

The speed of the comparator is more than needed for the application. Therefore it is interesting to study the optimization and bias current reduction in the comparator as a trade-off for speed and delay.

The layout techniques used focused on the reduction of miss-match and safety, there is room for some area reduction in the interconnections.

It is also desirable to assess the amplitude detection accuracy as required by [2], its deviation must be below 5%. If the detection threshold is not within this range several approaches can be used to modify the circuit in order to comply with the requirement. One possible solution is to use the offset control mechanism only to reduce offset and not to filter out noise. The noise rejection is done by having a reference voltage for the comparator different than that of the filter. This reference voltage can be approximately the same of the filter plus 20mV so only signals with an amplitude of 20mV will produce detections, this will bring the accuracy within the required range. Other designs can be employed as well, to determine the best approach a further in-depth study must be done.

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Appendices

Appendix A

Article submitted and accepted at Iberchip 2018, Puerto Vallarta, Mexico.

A 100nA Cardiac Sensing Channel with automatic offset correction

Rafael Puyol, Matías Miguez

***Abstract*—A complete cardiac sensing channel with a current consumption of just 100nA was designed. The system includes an automatic offset correction scheme that reduces offset to -400μV, with σ=1.4mV according to Montecarlo simulations. A comparator using the adaptive bias current generator technique was designed and can detect 10mV changes in the input in 2.28ms with a consumption of just 45nA (considering 20 detections per second). The sensing channel has 32 different threshold values that can be selected and works correctly for supply voltages between 2.0V and 3.3V. The circuit is designed in a 0.6um HV-CMOS technology.**

***Index Terms*—Cardiac Sensing, Low power design, automatic offset reduction.**

I. Introduction

PACEMAKERS are still the most used implantable medical devices (IMD), though in recent years many different devices for various pathologies are being developed [1][2][3]. Despite the first pacemaker being installed more than 50 years ago, there is still research in new ways to implement its function, and in increasing battery life by reducing power consumption. All advanced implantable medical devices have the basic blocks that are shown in fig. 1. Each IMD has a central intelligence that controls how the device works, telemetry to communicate and setup the device, a stimulation block as an actuator and finally some sensing system to gather information about the patient and/or his environment. The usual pacemaker must at least sense both the auricular and ventricular natural electric activity to determine if a stimulus is required or if the heart is working correctly and it's not necessary. This requires two sensing channels, each able to detect the electric pulse generated when the hearts beat. This works focuses on this sensing block for a pacemaker, but the design methodology could be used for other implantable devices, to sense other electrical signals of the body, for example ENG signals.

A. Sensing Block Requirements

The main requirements when designing a circuit for an implantable device is safety and low power consumption. The standard requirements for implantable medical devices is that if one component fails, no harm must be subjected to the patient.

In this design, the same safety guidelines as in [4] were used. A sensing block must be connected to the electrodes, and it has a digital output that is activated when the heart has beat. Generally, this is implemented with an amplifier that is connected to a comparator, that provides the digital output. Because each heart is slightly different and the heart/electrode interface is complex and may evolve in time, the sensing block must have different programmable values of detection threshold. From the standard [5], these thresholds are defined using the Tokyo signal. The complete requirements are shown in table I.

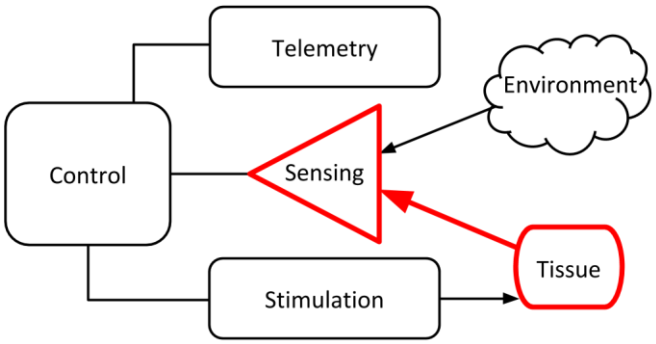

Fig. 1. Basic blocks of all implantable medical devices. This works focuses on the sensing of the signals form the tissue (red).

Some previous work, show sensing blocks consuming 0.74uA [6] and around 1uA is standard [7]. In this work, a consumption of just 100nA was specified for the complete sensing block.

TABLE I
SENSING BLOCK REQUIREMENTS

Quantity	Value
Supply Voltage	2.0V to 3.3V
Minimum threshold Value	200μV Tokyo signal [5]
Maximum threshold Value	10mV Tokyo signal [5]
Detection time	< 5ms
Consumption	< 100nA

II. Designed Sensing Block

The basic topology of the designed block is shown in fig. 2. The signal first goes through a Gm-C filter/amplifier and then into the comparator that provides the digital output. The threshold of the system is modified by changing the gain of the filter-amplifier with 5 bits allowing for 32 different threshold values. One technique to achieve low offset, is trimming the circuit after fabrication, but this is not always available. For these last cases, a digital automatic self-calibration was included in this block. This offset reduction is

R. Puyol and M. Miguez are with the Departamento de Ingeniería Eléctrica, Universidad Católica del Uruguay (email: rpuyol@ucu.edu.uy).

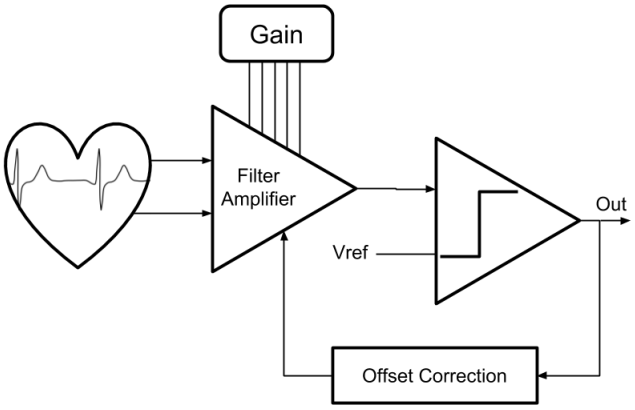

Fig. 2. Sensing block schematic. The sensing threshold is adjusted using the 5 bits of the Gain block. The output of the comparator is used to adjust the filter amplifier when the offset correction is active.

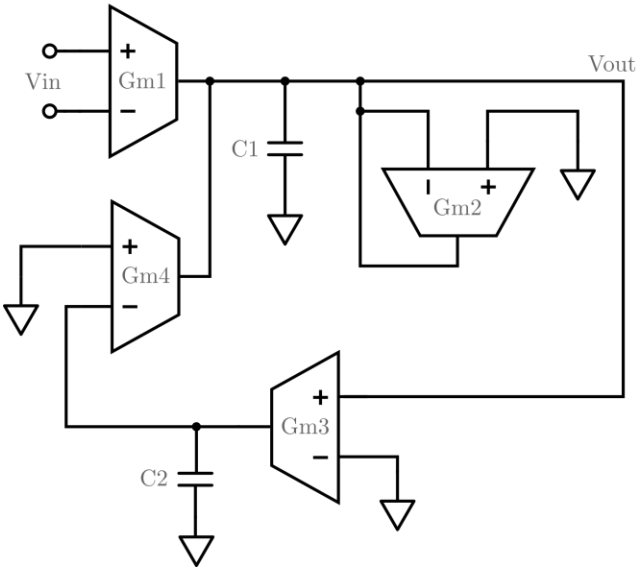

Fig. 3. The architecture of the 1st order bandpass filter implemented using transconductance amplifiers (Gm) and integrated capacitors (C).

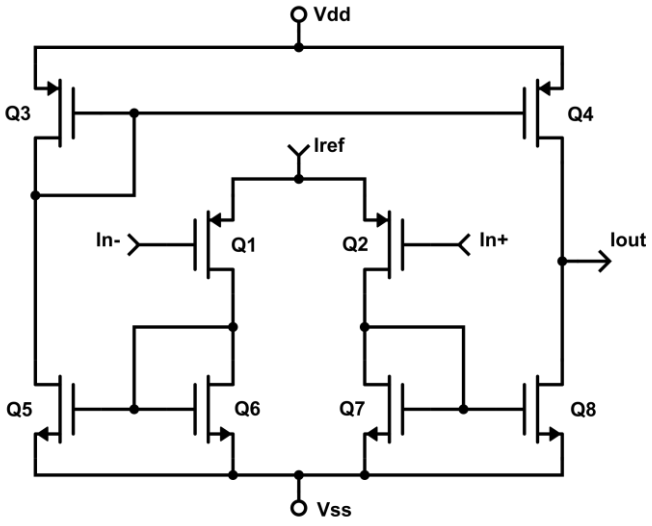

Fig. 4. Schematic of the OTA used in the filter amplifier. All 4 Gm use the same architecture, but with different polarization current and transistor sizes as shown in Table II.

done when the circuit is first powered on, but can also be repeated if needed.

A. Gm-C filter amplifier

The amplifier selected topology is shown in fig. 3 and is similar to [8]. The circuit implements a first order band pass filter, using four symmetrical transconductance amplifiers (OTA) to implement each Gm. The schematics of the Gm is shown in Fig. 4, and the transistor sizes in Table II. The capacitances of C1 and C2 are 1.7pF and 40pF respectively. The gain of the amplifier is modified by increasing or decreasing the polarization current of the Gm1. This is implemented by turning on/off 5 mirror transistors of different sizes (1, 2, 4, 8, 16). The amplifier maximum gain is 56V/V, with an amplifying band between 60Hz and 290Hz. Total consumption of the amplifier is less than 50nA in its worst case.

TABLE II
OTA TRANSISTOR SIZES

	Gm1	Gm2	Gm3	Gm4
Q1 / Q2	W=160µm L=32µm	W=100µm L=20µm	W=100µm L=20µm	W=100µm L=20µm
Q3 / Q4	W=80µm L=80µm	W=20µm L=20µm	W=20µm L=20µm	W=20µm L=20µm
Q6 / Q7	W=40µm L=25µm	W=80µm L=40µm	W=20µm L=35µm	W=20µm L=40µm
Q5 / Q8	W=40µm L=40µm	W=20µm L=40µm	W=20µm L=40µm	W=20µm L=40µm
Iref	38.75nA – 1.25nA	2nA	0.5nA	0.5nA

B. Comparator

Several comparators designs were evaluated to achieve the minimum power consumption and adequate detection speed. The architecture selected, shown in Fig.5, is based on [9] which achieves low consumption by means of adaptive bias current generator (ABCG) [10]. The speed of this comparator is heavily affected by the bias current of the input differential pair. With the use of ABCG a greater bias current is achieved only when a differential signal is present at the inputs. The comparator consists of differential pair (Q1, Q2), an ABCG with hysteresis control, two latches and a pair of inverters. Two positive feedback loops are used for the current generation each with a switch in series (Q9, Q10). When a comparison is finished the latches turn the switches off and the bias current decreases to its resting value. Total consumption of the simulated comparator was in average 45nA, when there was one detection every 50ms.

C. Digital calibration

To modify the offset of the filter amplifier a set of 5 digitally-controlled current mirrors is placed in parallel with C2 in figure 3. The changes in offset are equidistant for consecutive words.

The digital calibration circuits controls the offset tunning mechanism. To perform a calibration the inputs of the filter are shorted to ground and both the offset correction and gain are set to their maximum value. The negative input of the comparator is always connected to fixed reference voltage. If

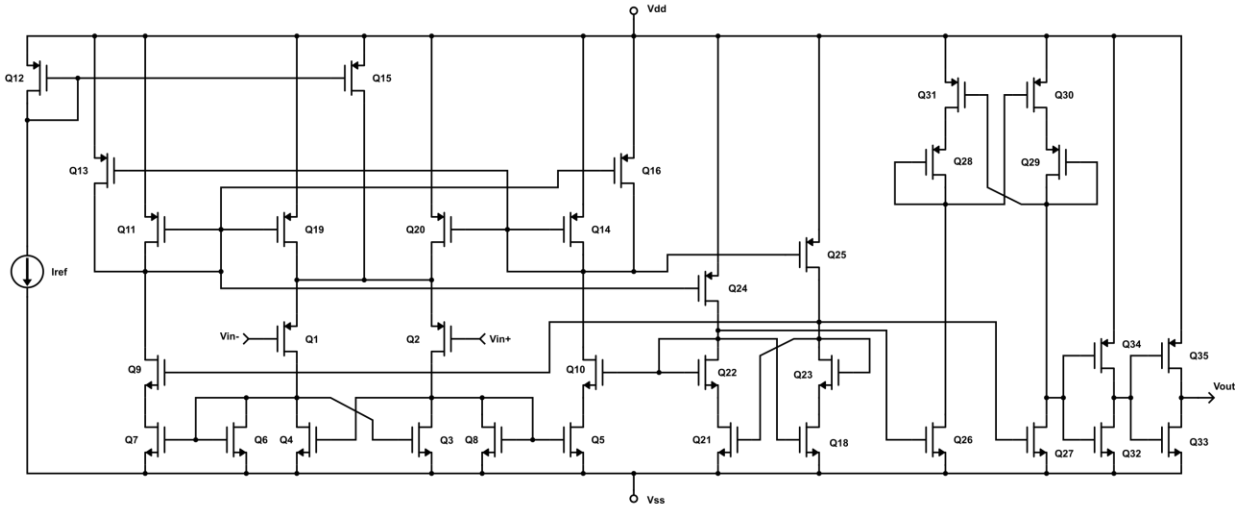

Fig. 5. Schematic of the implemented comparator. The ABCG improves the speed of the comparator while maintaining low power consumption.

the comparator does not switch its output before a given timeout the offset value is decreased one step and the timeout cleared, this process is repeated until the comparator changes its output. After the detection the calibration value is stored in 5 D flip-flops and the calibration phase stops, resuming the circuit normal operation. The detection threshold of the comparator is time-dependent so the step time can be increased to minimize this issue. For most applications this is done with a very low frequency, so the calibration time is not significant.

III. Simulated Results

The system was simulated for several working conditions. Fig. 6 shows the process of calibration and the sensing of the minimum value of Tokyo signal. The system calibrates itself in less than 1 second. During the calibration process the filter is disconnected from the tissue, and short-circuited. After the calibration is finished the system is ready to sense.

Using Montecarlo simulation, the offset of the complete channel was estimated. Fig. 7 shows the distribution of the final offset for the calibrated system, showing it is well below the minimum expected detection value (10mV at the input of the comparator). Without calibration the offset has a bigger standard deviation, and in some cases exceeded 10mV. This was reduced after calibration, showing that the system is working correctly.

For the filter amplifier, the maximum gain simulated using Montecarlo has an average of 56.3 V/V, σ=4.2V/V, while the 3dB frequency poles are 61Hz, σ=4.3Hz and 290Hz, σ=10Hz. Fig. 8 shows different gain values of the filter amplifier, to change the detection threshold. The detection time of the comparator was simulated for a signal difference of 10mV and its distribution is shown in Fig. 9, with an average value of 2.28ms, σ=0.26ms that is always less than the required 5ms.

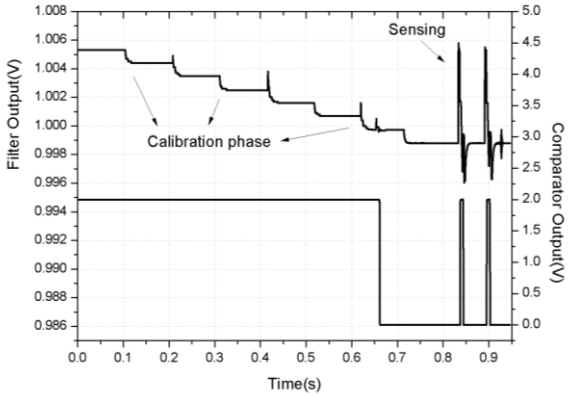

Fig. 6. Transit simulation of the turning on of the comparator. At the beginning the calibration phase is performed. The input is short-circuited during this phase. Later two Tokyo signals of 200μV are applied and detected.

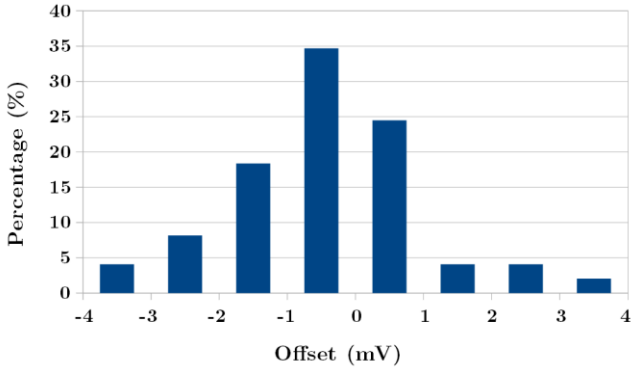

Fig. 7. Distribution of system offset using calibration. Offset is -400μV, with σ=1.4mV.

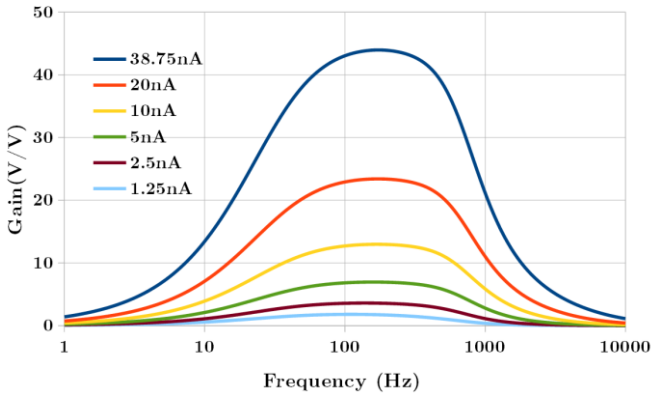

Fig. 8. The gain of the filter amplifier is modified to define different thresholds for the sensing block. The different filter amplifier responses for a few of the different polarization current is shown.

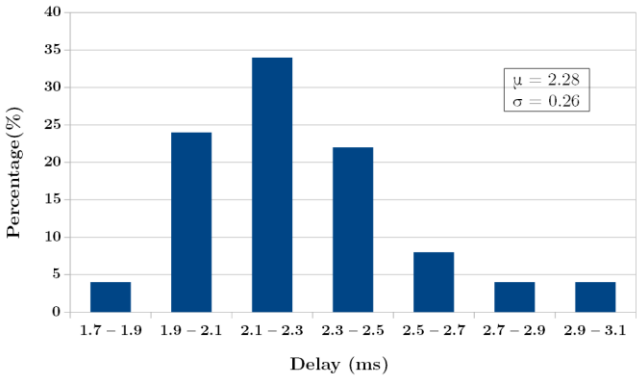

Fig. 9. Detection time for the implemented comparator. The detection time is 2.28ms, σ=0.26ms and is always less than the required 5ms.

IV. Conclusion

A complete sensing block for cardiac signals, suitable for a pacemaker, was designed simulated and is currently under fabrication for further testing. The complete system has a current consumption of just 100nA and implements an automatic calibration system to reduce offset.

Acknowledgment

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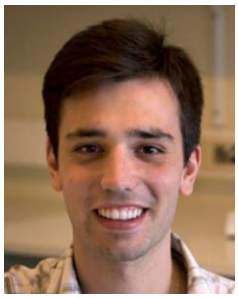

Rafael Puyol (GSM'14) received his degree in electronic engineering in 2013 from Universidad Catolica del Uruguay (UCU). In 2012 he joined the team at the Department of Electrical Engineering at UCU working on the study of flicker noise and low power microelectronic circuits. Since 2013 he is with BQN where he is actively involved in embedded systems.

Matias Miguez (M'08) received his PhD degree in Electronics Engineering from the Universidad Nacional del Sur, Bahia Blanca, Argentina in 2016 and his MSc and Graduate degree in Electronics Engineering from the Universidad Católica, Montevideo Uruguay in 2008 and 2005 respectively. He has also received a Graduate degree in Physics from the Universidad de la República, also in Montevideo, Uruguay in 2007.

In 2005, he joined the Electrical Engineering Department, Universidad Católica, Montevideo Uruguay. Since 2005 he has been involved in research projects in the field of CMOS analog design for low power applications.